Enabling Scalable Silicon Photonic Circuit Design and Fabrication

INVITED TALK, OECC 2015

Xu Wang, James Pond, and Jackson Klein
Lumerical Solutions, Inc., Vancouver, Canada

Andy Eu-Jin Lim, Kok Kiong Chen, and Guo-Qiang Lo
Institute of Microelectronics (IME), A*STAR, Singapore

Outline

Introduction

Silicon photonic design & simulation

IME PDK

- Compact model library (CML)

Example

Conclusions

Introduction

Silicon photonics offers many opportunities

edX course | Silicon Photonics Design, Fabrication and Data Analysis

- scalable
  - high-index contrast -> compact
  - a variety of devices -> high functionality
- low cost & high volume
  - CMOS manufacturing facility
- many applications
  - optical interconnects (data centers, telecom, HPC, …)
  - sensing (biological, chemical, …)

Circuit complexity continues to grow

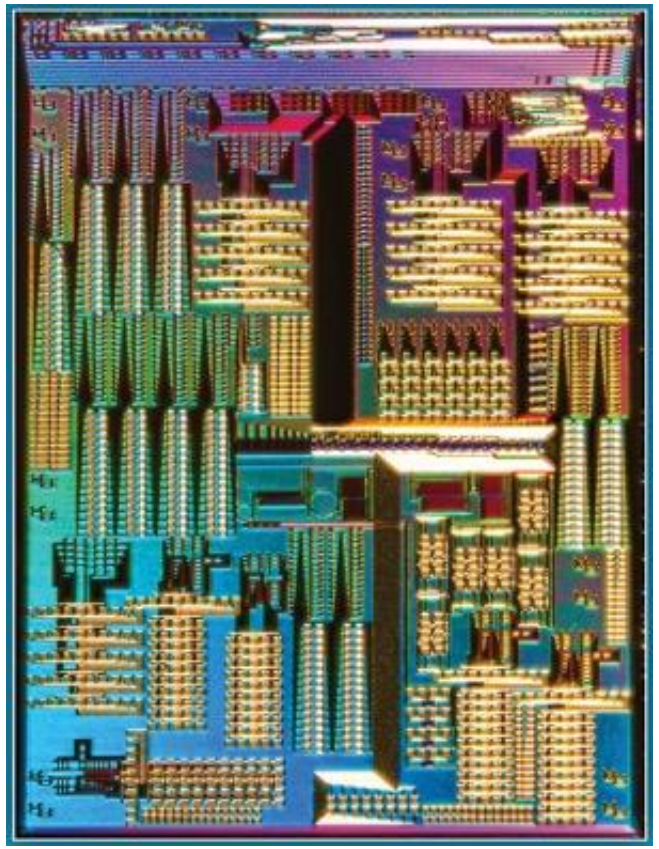
- Full design flow solutions are emerging
  - EDA tools + photonic simulation technologies
- Si photonic process design kits (PDKs) are emerging

Introduction

Fabless model and foundry

- Multi-project wafer (MPW) services
- Wide range of reliable components available
- Packaging
- Prototyping
- Path to mass production

Book: Silicon Photonics Design



SiEPIC-IME chip, including active components such as modulators

IME's Silicon-Photonics Industry Engagement Mode & Status

1-to-1 (customized)

MPWs (through IME or partners, e.g.,)

CMC MICRO SYSTEMS

Institute of Microelectronics, A*STAR

Active Device Library

Passive Device Library

Packaging

Institute of Microelectronics, A*STAR

Silicon Photonics Platform

- Waveguide systems:
  - Si waveguides
  - SiN waveguides
  - SiON waveguides
  - Suspended silica waveguides
- Si Modulators
- Ge Photodetectors
- Ge APDs
- Thermo-optic devices
- Vertical couplers
- Edge couplers (Deep trench)
- Packaging
- Combinations* of the above (*where compatible)

Institute of Microelectronics, A*STAR

Prototyping / Small Volume Production

IME, A*STAR

GLOBAL FOUNDRIES

Path for mass production (Ready 2015)

Si photonics design

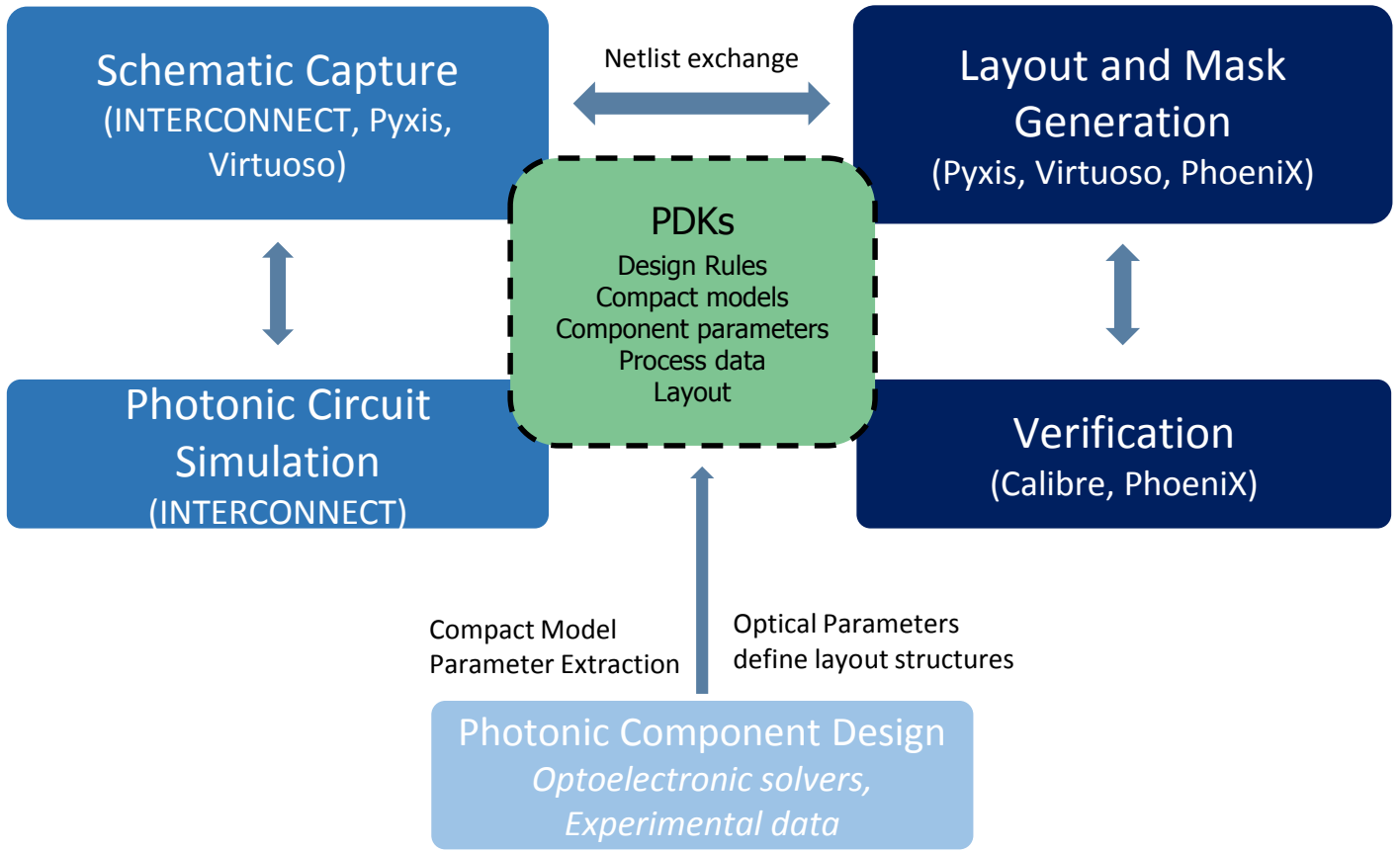
Si photonics design is less mature than electronic design

- Typically based on highly customized, user-specific component libraries
- The PICs are often designed and laid out manually
- Leads to errors and multiple, expensive design iterations

Solution

- Adopt workflows like those in the fabless CMOS semiconductor space
- The fundamental components are reliably defined for a specific process
- Complex systems can be built upon that library of components
- Requires reliable simulation tools and models

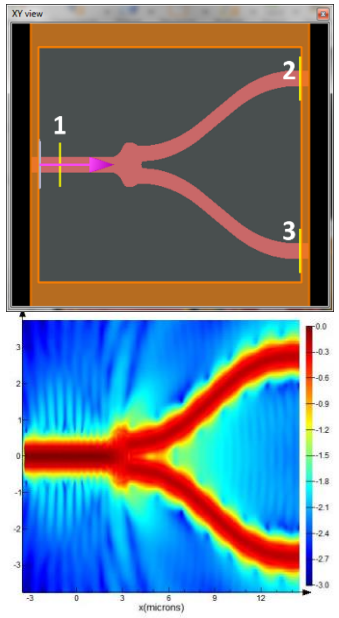
Unified work flow for Si photonics design

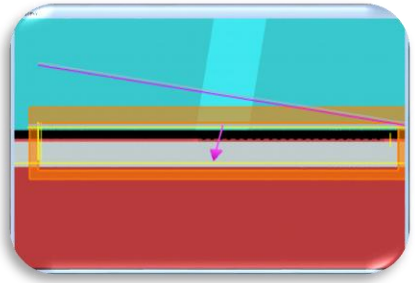


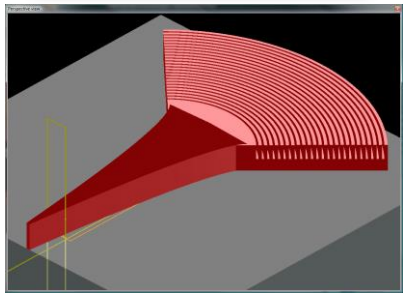
Si photonics component level design

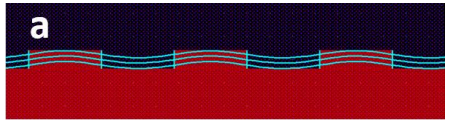
Component design tools are relatively mature

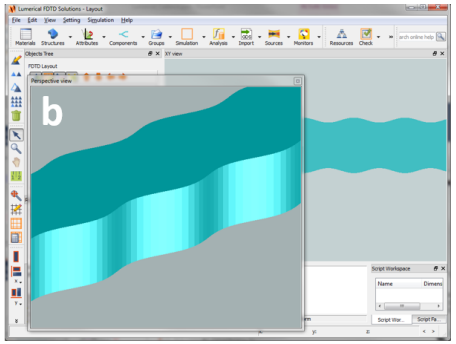
- Physics-based solvers:
  - Optical: solving Maxwell's equations, e.g., FDE, FDTD, EME…
  - Electrical: solving drift-diffusion and Poisson's equations

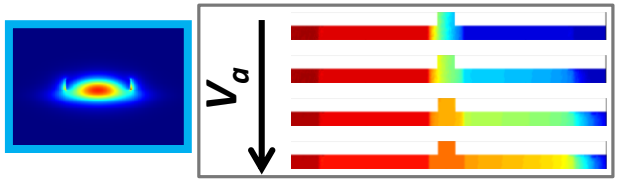


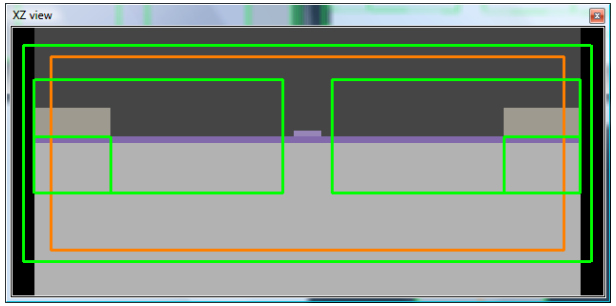


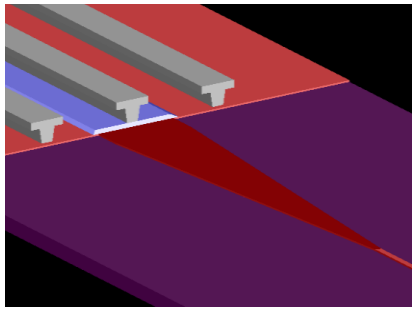


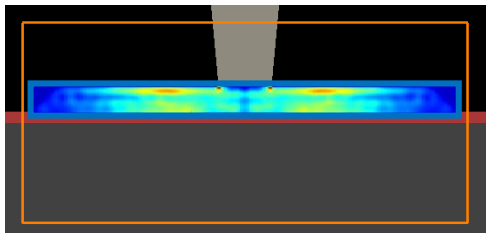












lumerical illuminating the way

Photonic circuit simulation challenges

Complex nature of optical signals

Both electrical and optical signals are required

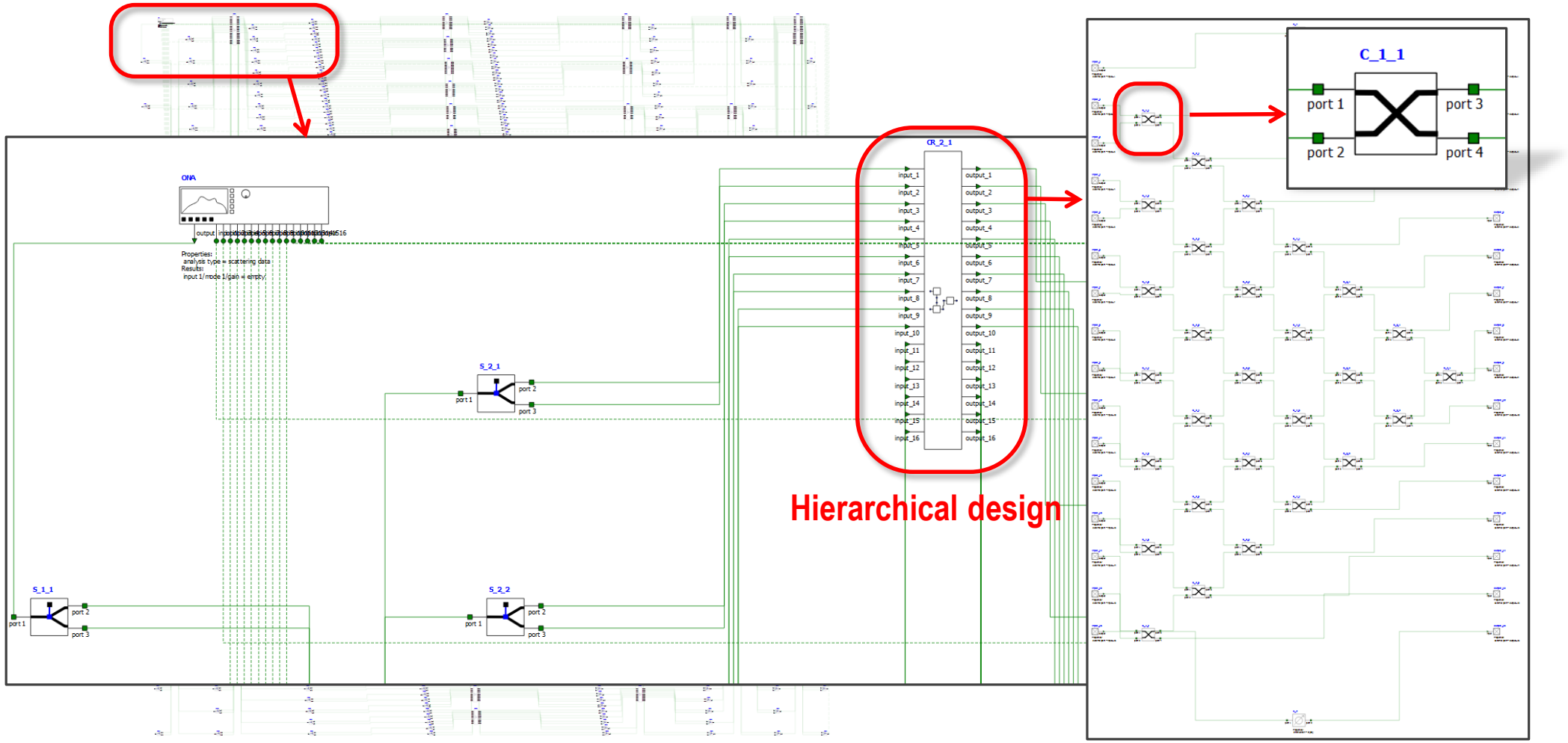
No standardized behavioral models exist

Frequency and time domain simulation are necessary

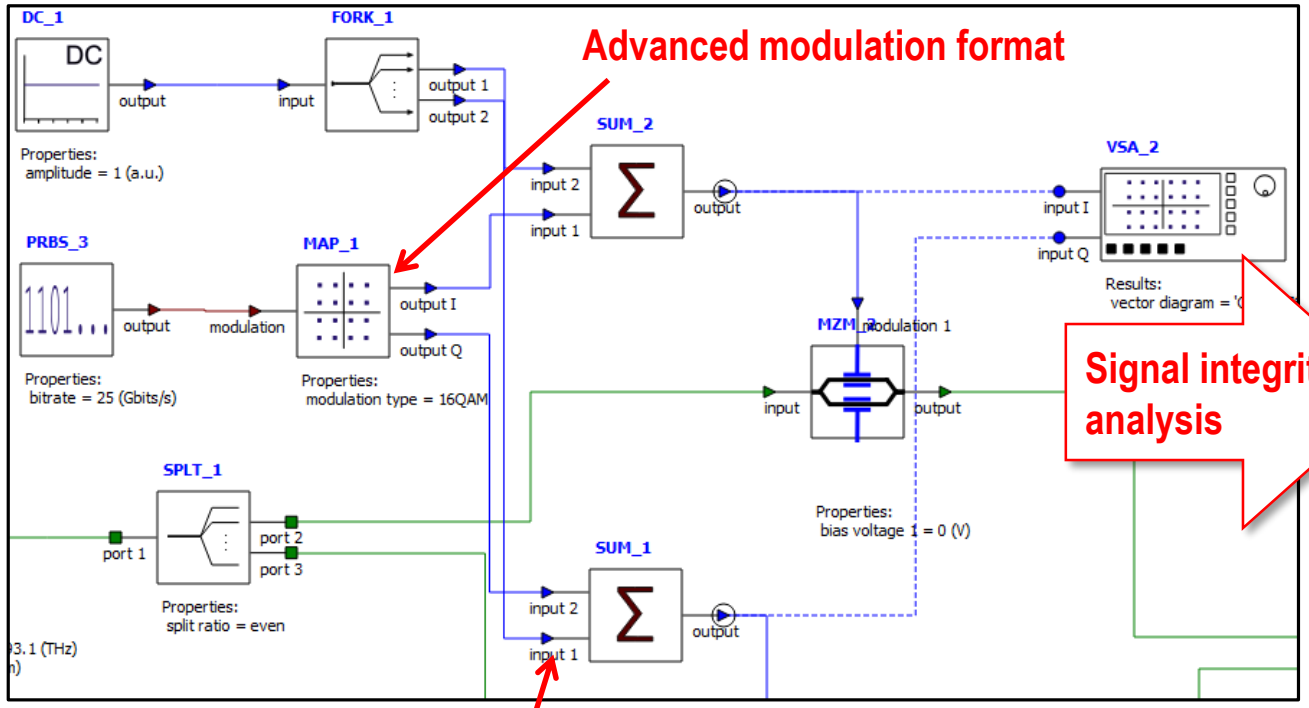
To meet these challenges, we must create a reliable compact model library

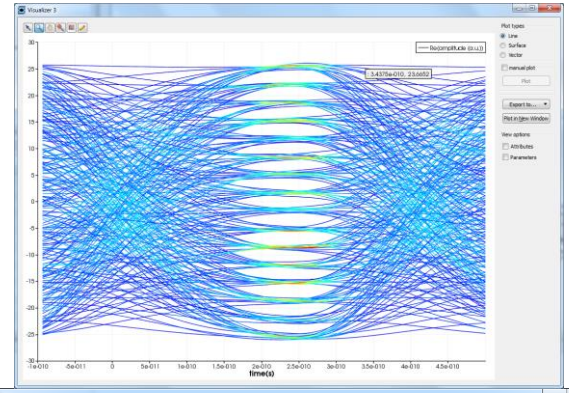
- Calibrated for a particular foundry process

Frequency domain example

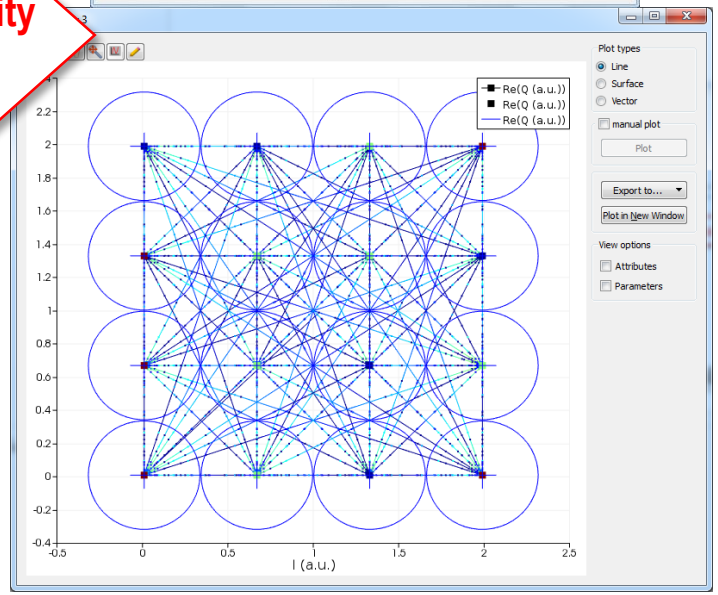


Time domain example

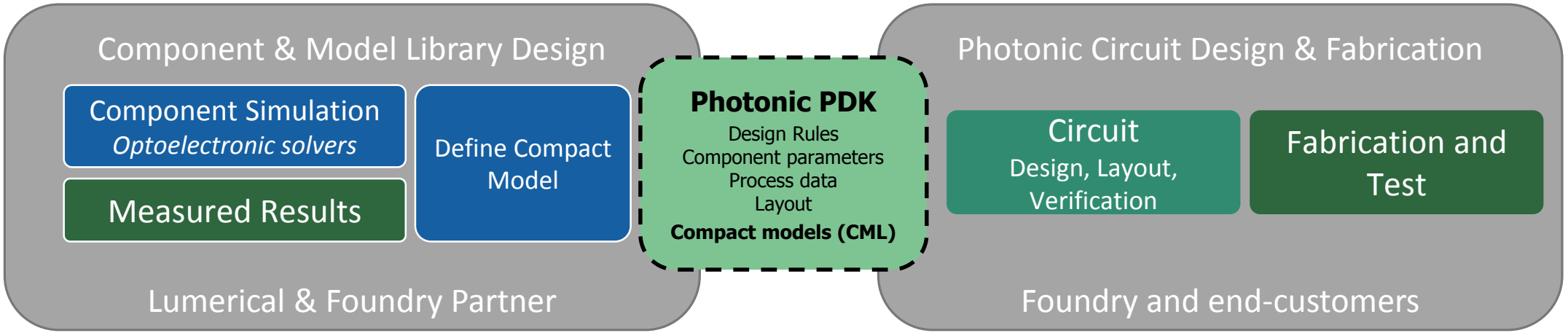




Signal integrity analysis



Why do we need a PDK?



IME PDK

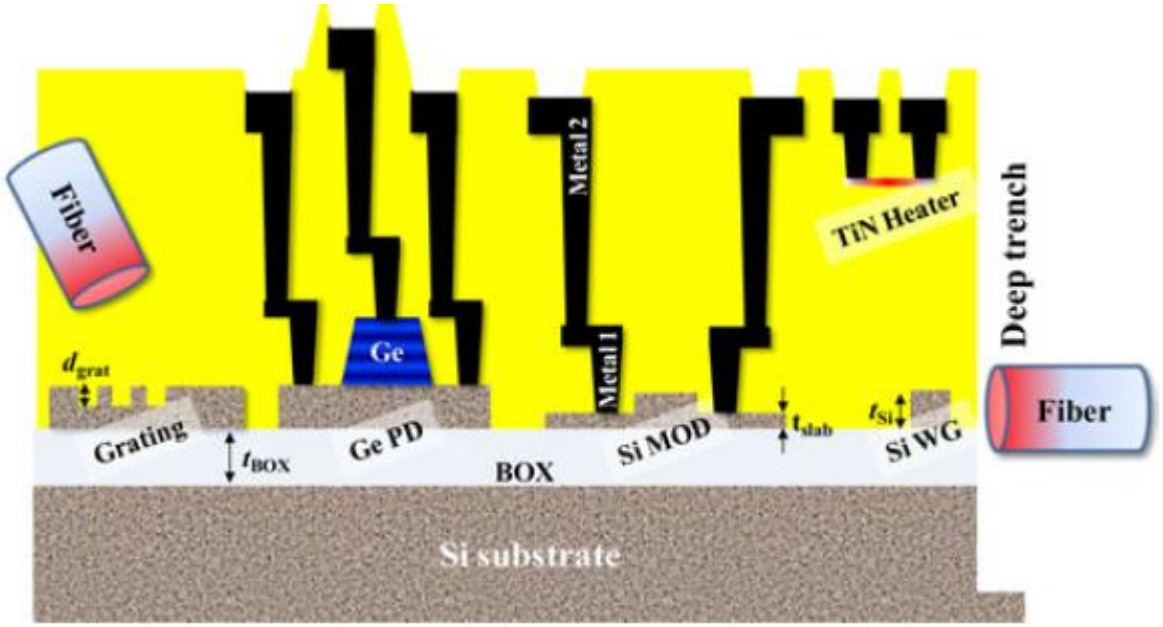
The IME PDK includes

- Device integration and process information
- Device building blocks
- Mask layout
- Design rules
- Process control monitoring structures

Now includes a CML developed jointly with Lumerical

IME process

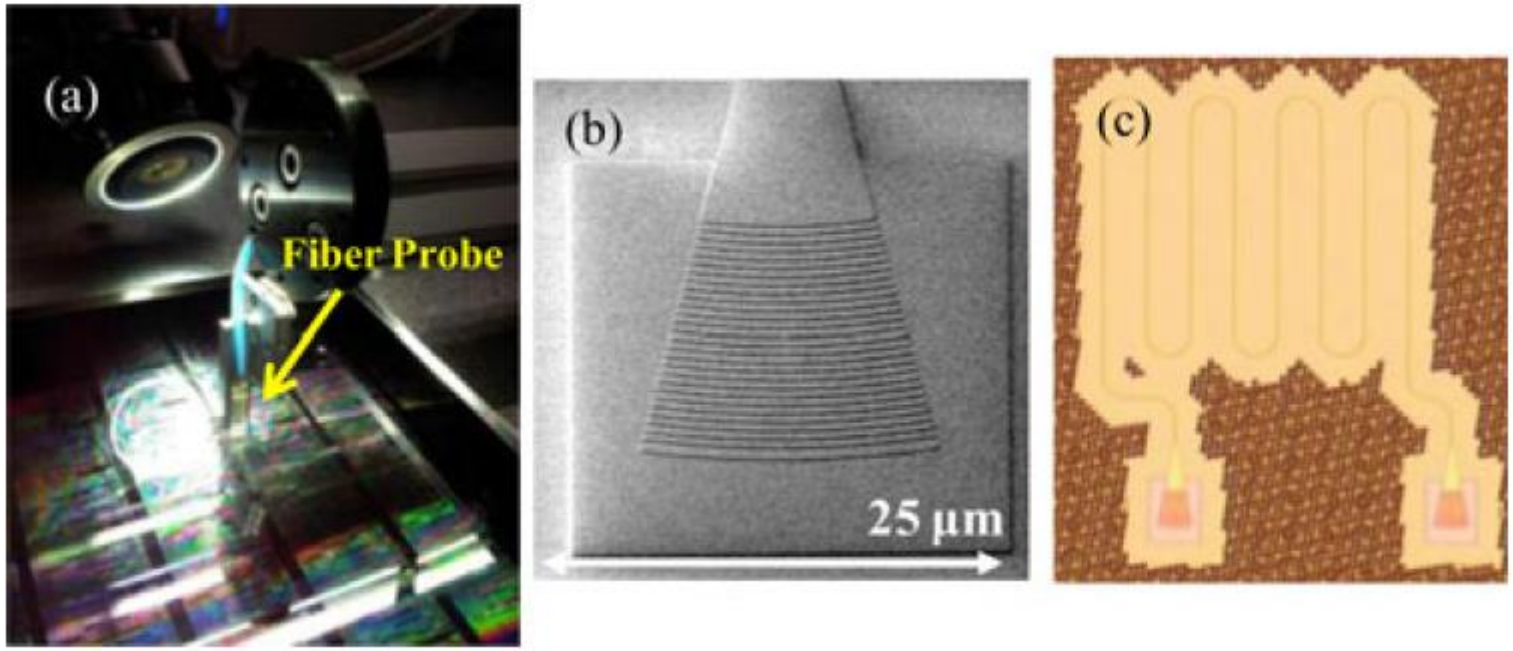
- 220 nm Si / 3 µm BOX SOI
- Partial Si etches of 70 nm and 130 nm
- Germanium (Ge) epitaxy
- Multiple ion implantation steps
- Two-level metallization
- TiN heater for thermal-optic tuning
- A final deep trench Si etch



Andy Eu-Jin Lim, et al., “Review of Silicon Photonics Foundry Efforts”, JSTQE vol. 20, no. 4, 2014.

IME components

Wafer-level test setup, grating coupler, waveguides

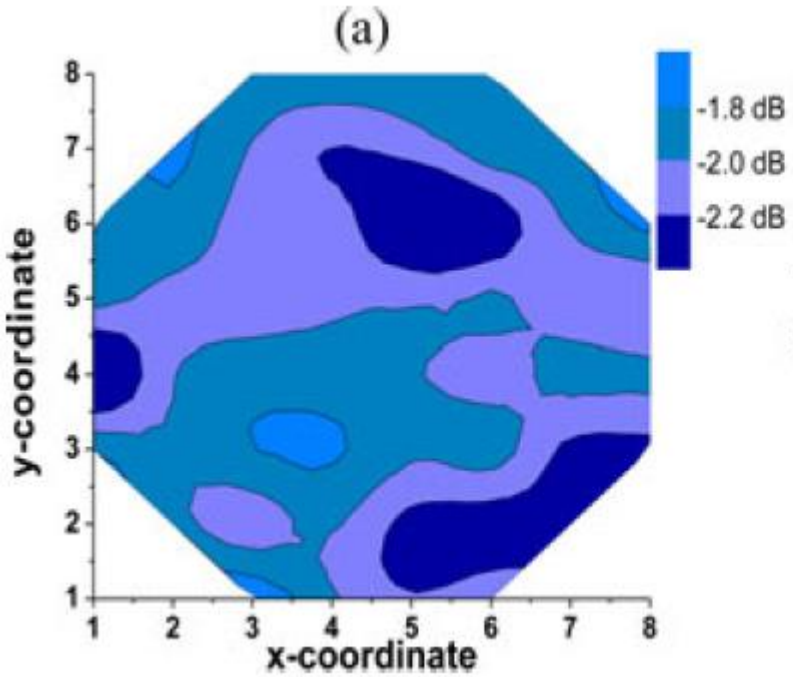


Andy Eu-Jin Lim, et al., “Review of Silicon Photonics Foundry Efforts”, JSTQE vol. 20, no. 4, 2014.

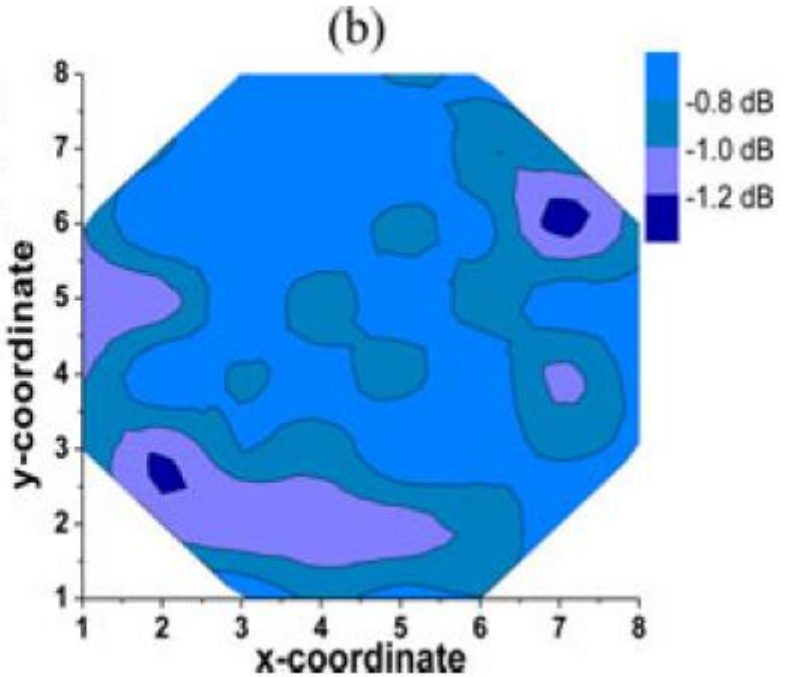
IME components

Excellent waveguide loss uniformity

Strip waveguide: ~2 dB/cm



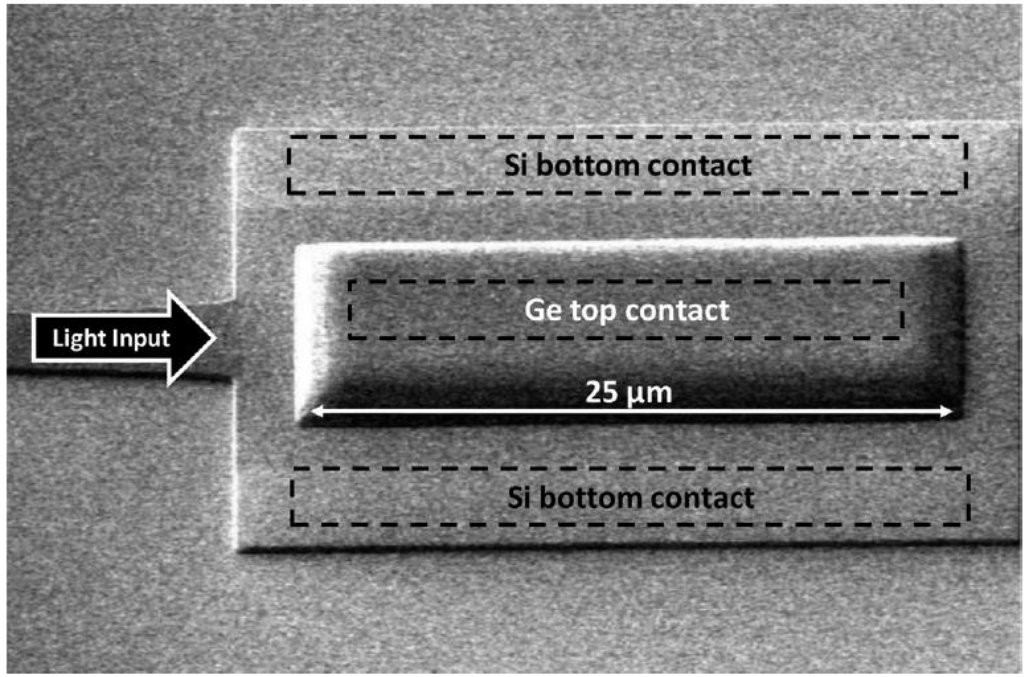
Rib waveguide: ~0.8 dB/cm

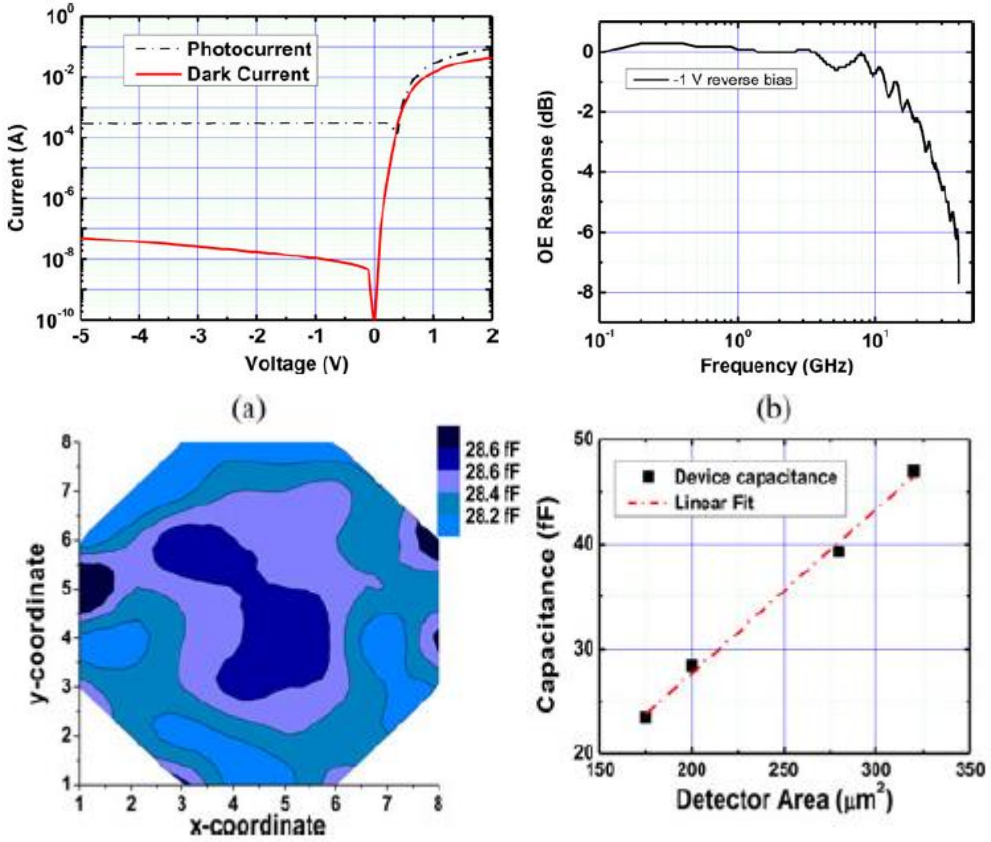


Andy Eu-Jin Lim, et al., “Review of Silicon Photonics Foundry Efforts”, JSTQE vol. 20, no. 4, 2014.

IME components

Photodetector

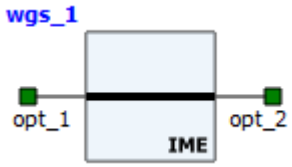


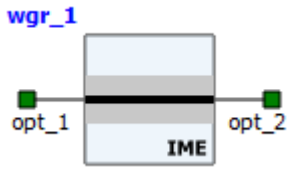


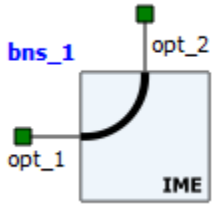
Andy Eu-Jin Lim, et al., "Review of Silicon Photonics Foundry Efforts", JSTQE vol. 20, no. 4, 2014.

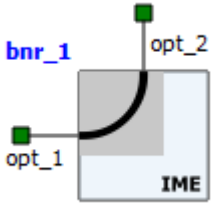
IME CML

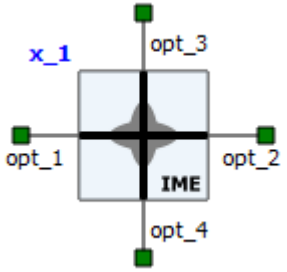
Waveguides



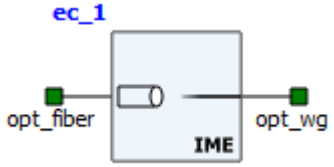


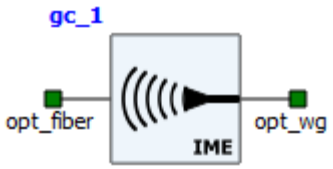


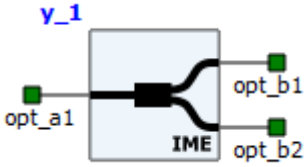


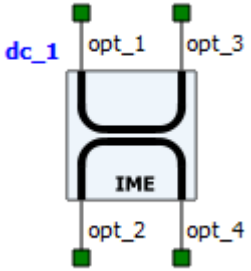


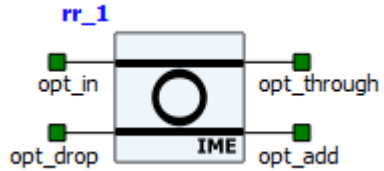
Other Passives



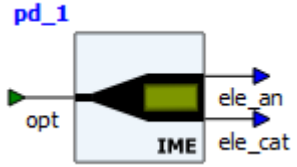


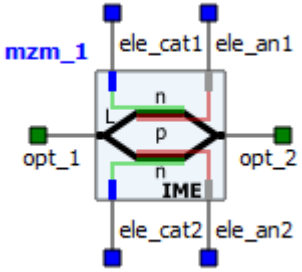


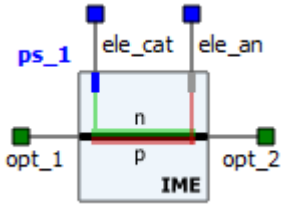


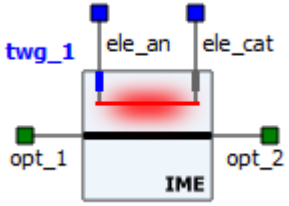


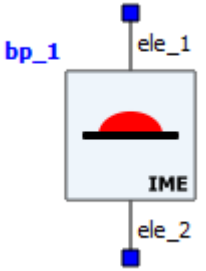
Actives











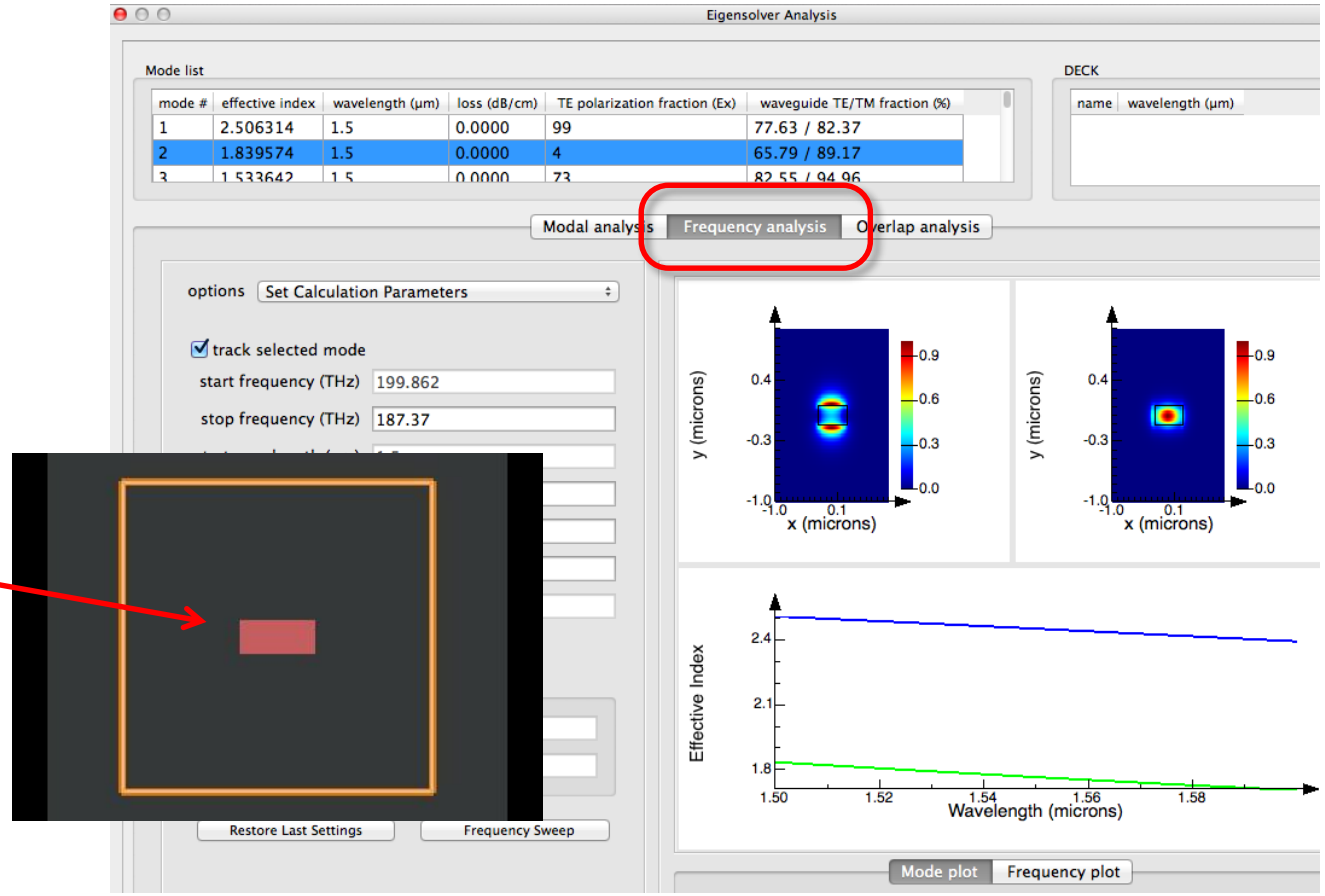
CML generation

Waveguides

Required:
- neff
- ng
- loss

Advanced:
- neff(λ)
- ng(λ) or dispersion
- multiple modes

Typical inputs from the fab:
- cross-section for FDE simulation
  - width, height (etch depth)
  - cladding material (air/SiO_2)
  - sidewall angle (if available)
- measured propagation loss
  - e.g., 2 dB/cm for strip WG

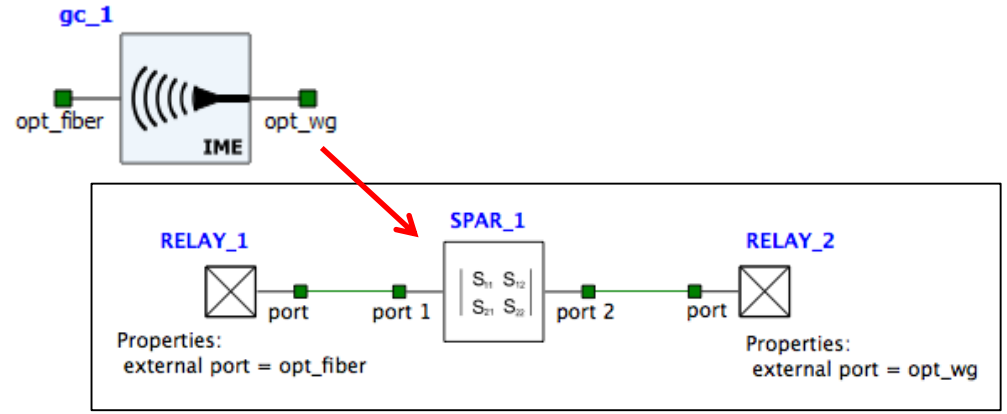


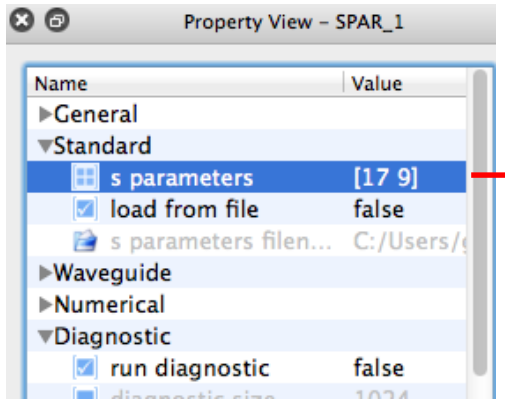
CML generation

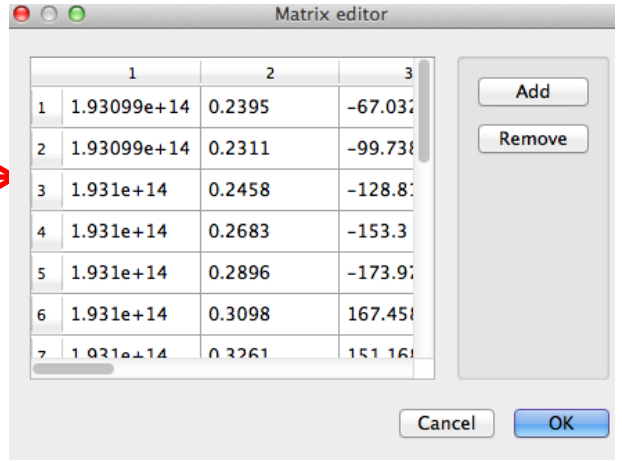
Other passive components

Required:
- S parameters

Typical inputs from the fab:
- measured transmission
- measured crosstalk or back reflection
- physical geometry for 3D FDTD simulation (if necessary)







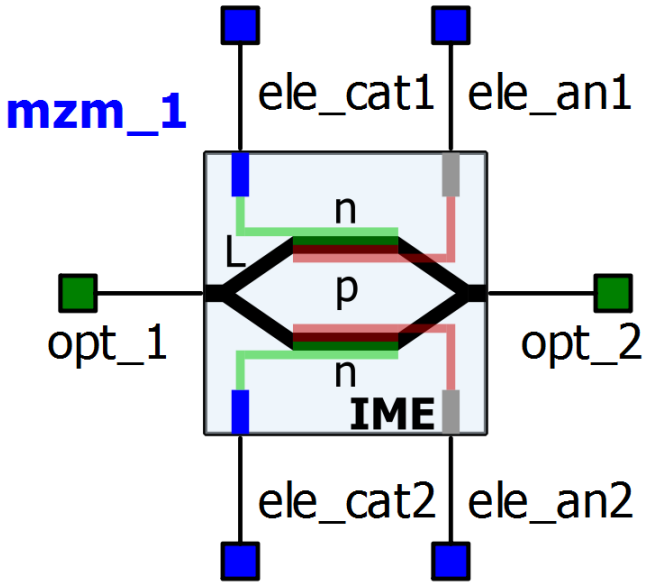
CML generation

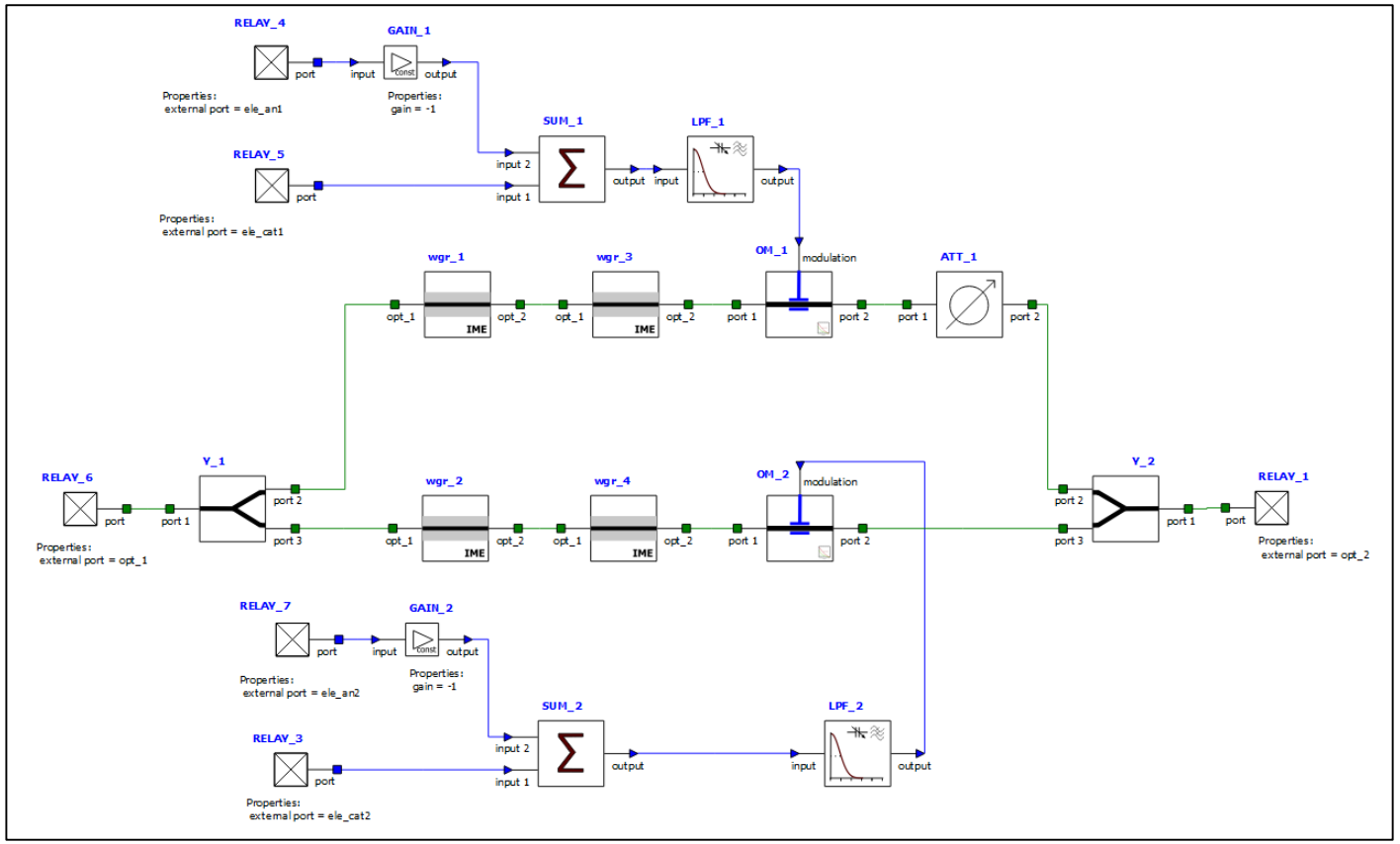
Active devices are often much more complicated

- Modulators
  - Phase shifter characteristics: neff(V), loss (V)
  - Transmission spectra vs. voltage
  - Modulation frequency response
  - Travelling wave data, …
- Detectors
  - Responsivity (as a function of λ)
  - Dark current (as a function of bias and temperature)
  - Modulation frequency response
  - Noise, …

CML generation

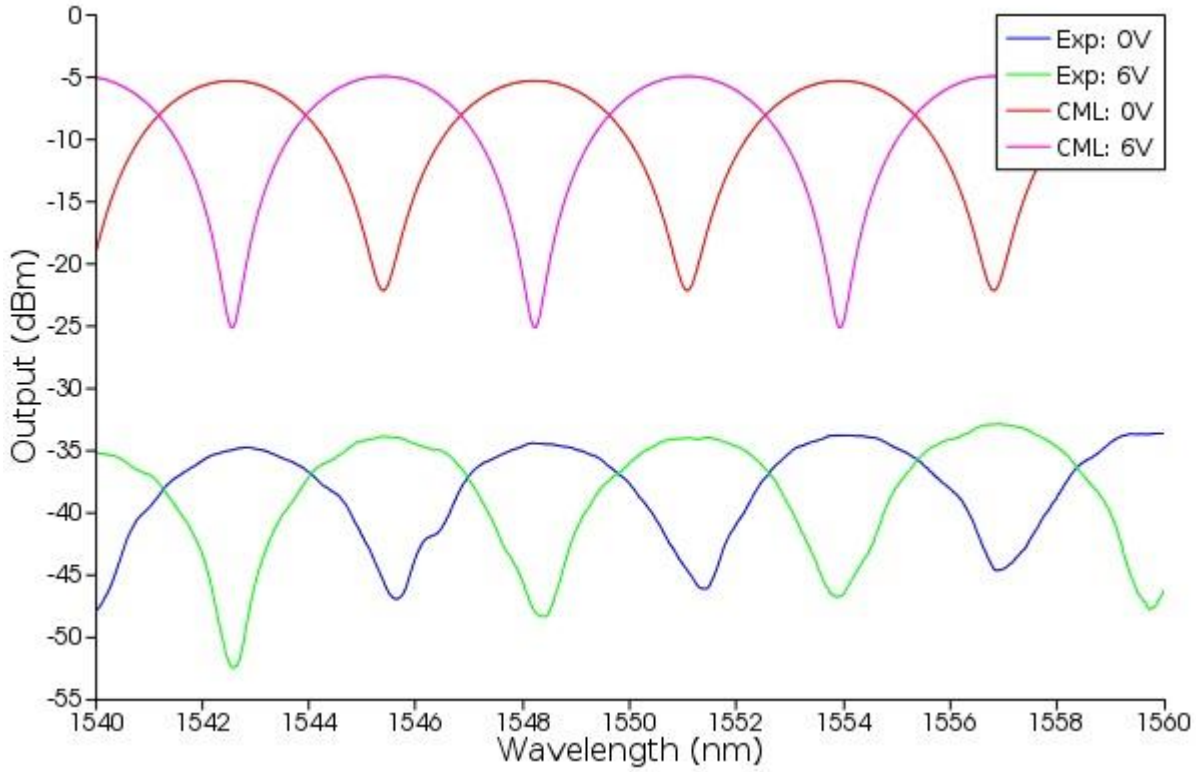
IME Mach-Zehnder Modulator





CML generation

IME Mach-Zehnder Modulator

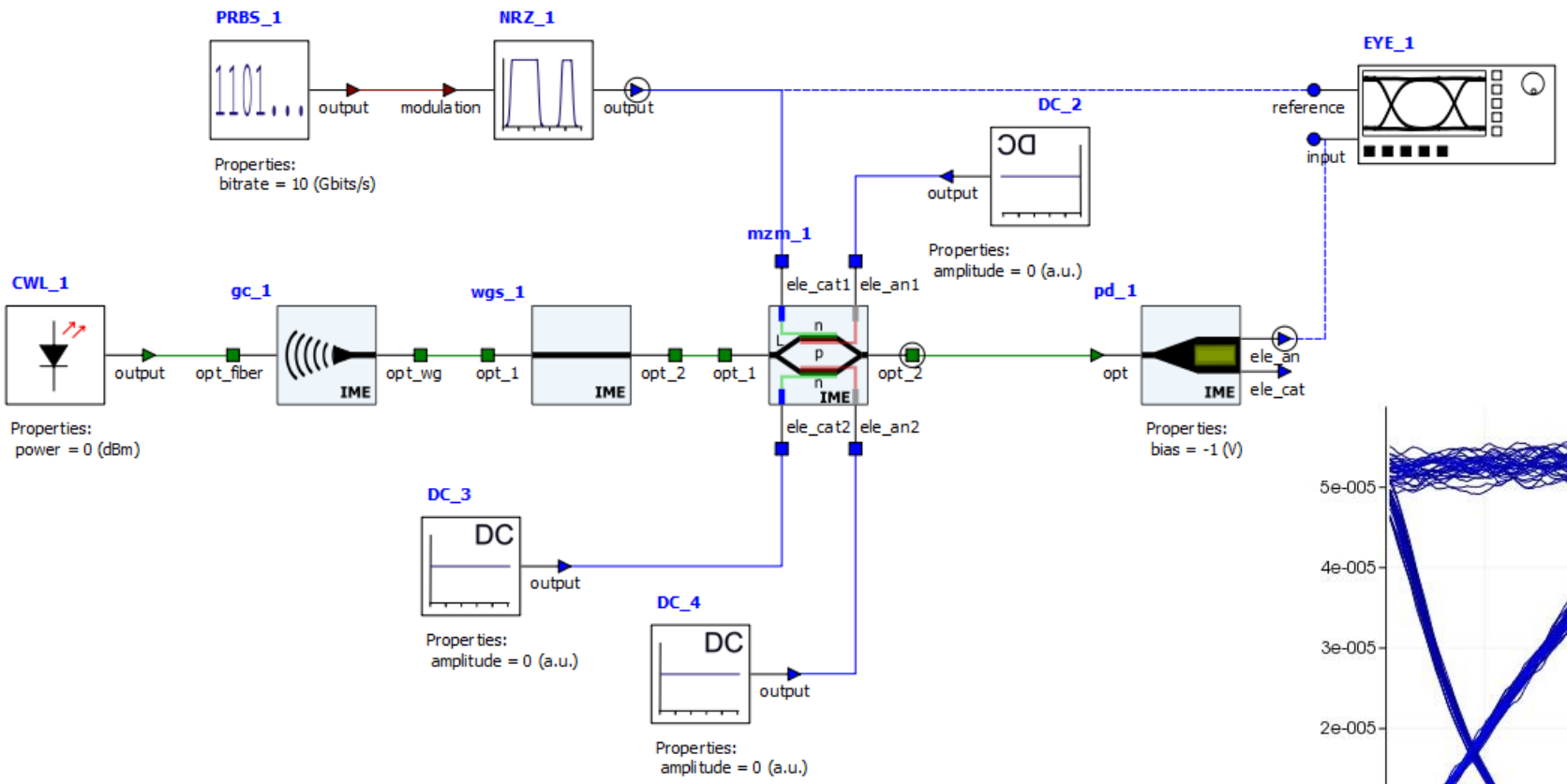


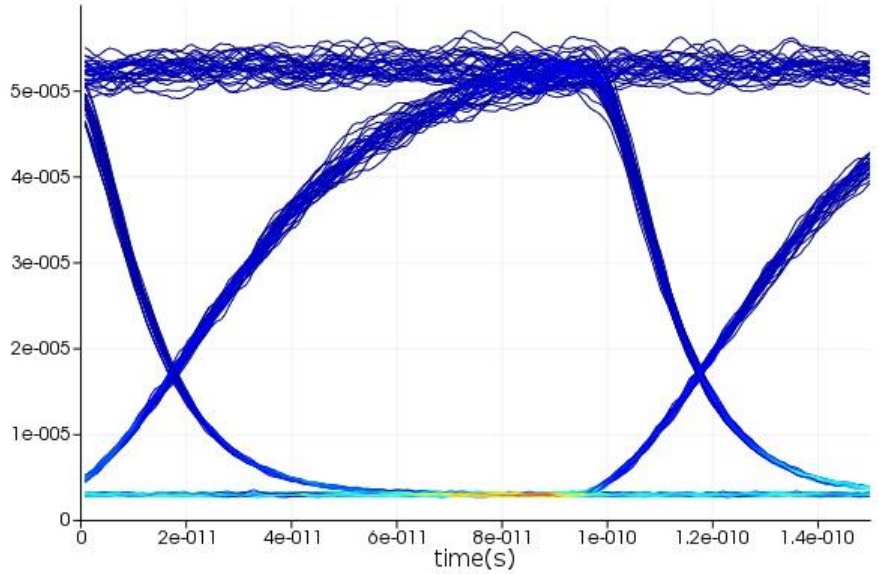
simulation

vs.

experiments

Example circuit using the CML





Conclusion

Silicon photonics offers many opportunities

- Low cost, scalable, high volume, …

Workflows must become mature like in EDA

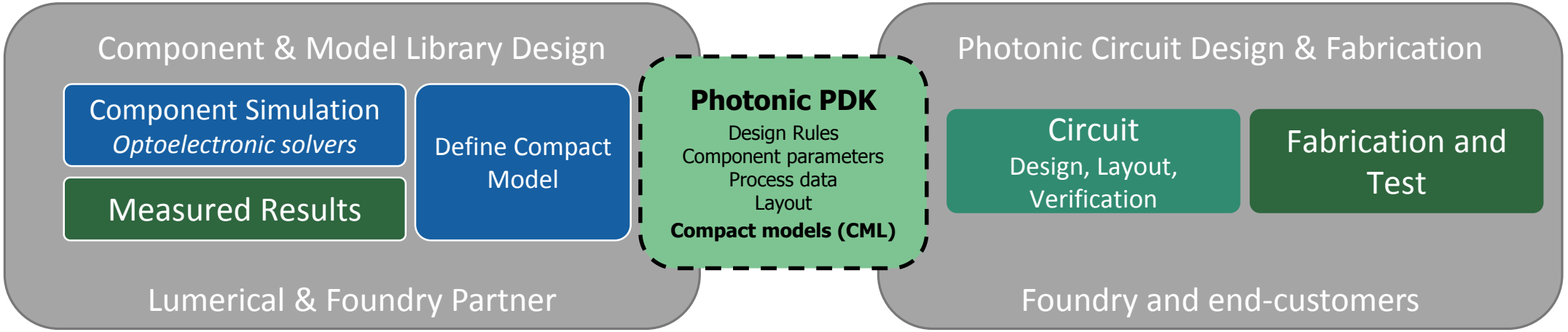
- Separation of component level design and circuit design
- Interface is the PDK
- Requires accurate circuit simulations with a calibrated CML

Many challenges with photonic circuit simulation

- We can create a CML that accurate represents component behavior
- Requires a combination of experimental and physical simulation results

IME and Lumerical have developed the first Si photonics foundry CML, available in the IME PDK.

Foundry Partners



To learn more, visit www.lumerical.com/foundry

Featured Foundry Partners

Sandia National Laboratories

A*STAR Institute of Microelectronics

https://www.lumerical.com/company/news/releases/sandia_partnership.html

www.lumerical.com

Connect with Lumerical




Contact Us

Questions? support@lumerical.com

Sales Inquiries: sales@lumerical.com

Contact your local Lumerical representative

Start your free 30 day trial today www.lumerical.com

lumerical illuminating the way