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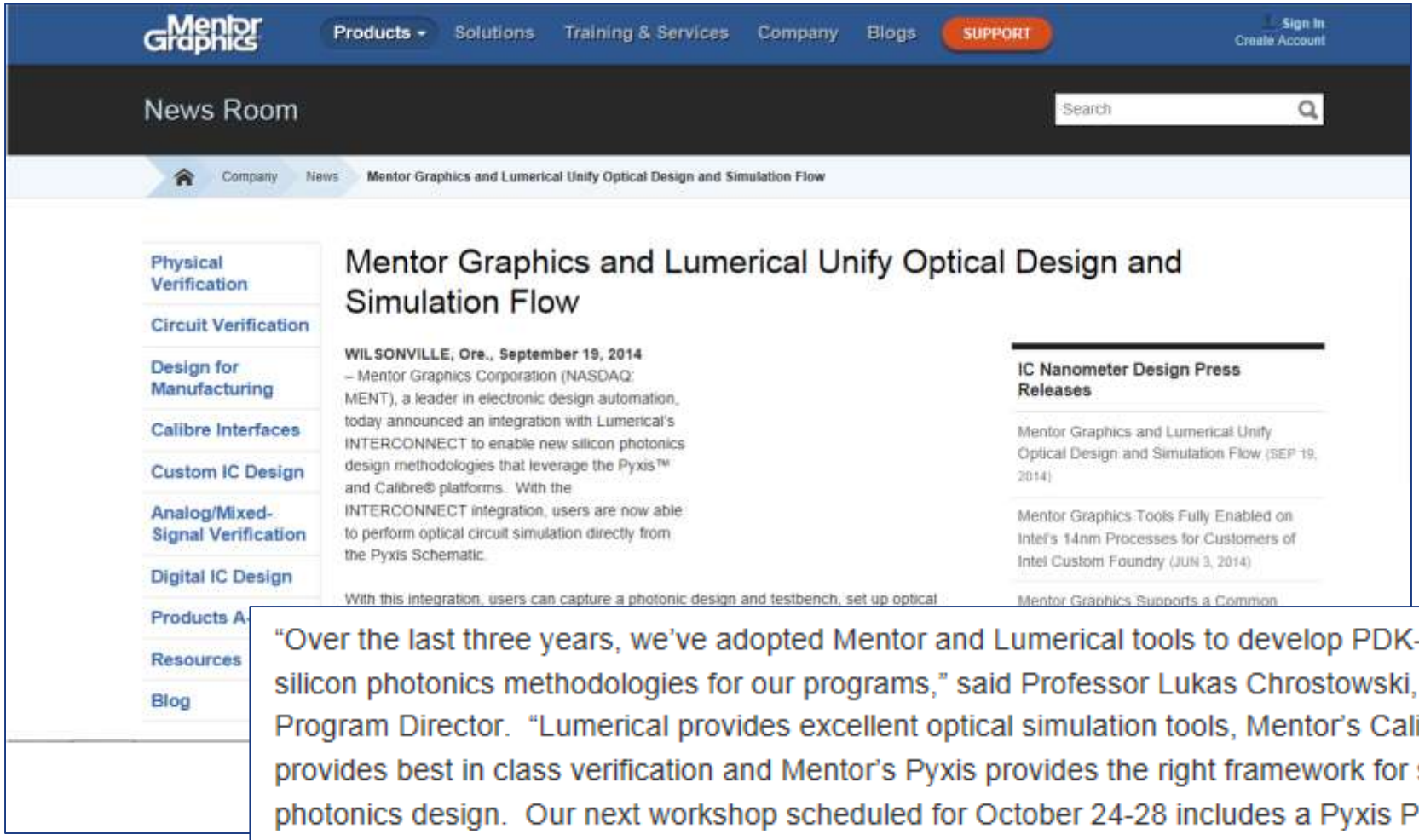
# Unified Design Flow for Silicon Photonics

40th ecoc
Cannes 2014

# Outline

- Silicon photonics flow introduction
- Photonic IC circuit simulation with INTERCONNECT
- PDK driven flow with Pyxis and Calibre
  - ↗ Design capture and implementation with Pyxis
- PDK driven flow with Pyxis and Calibre (continued)
  - ↗ Physical verification Calibre
  - ↗ PhoeniX Collaboration
- Photonics + CMOS
- Available PDKs

# What's new ?

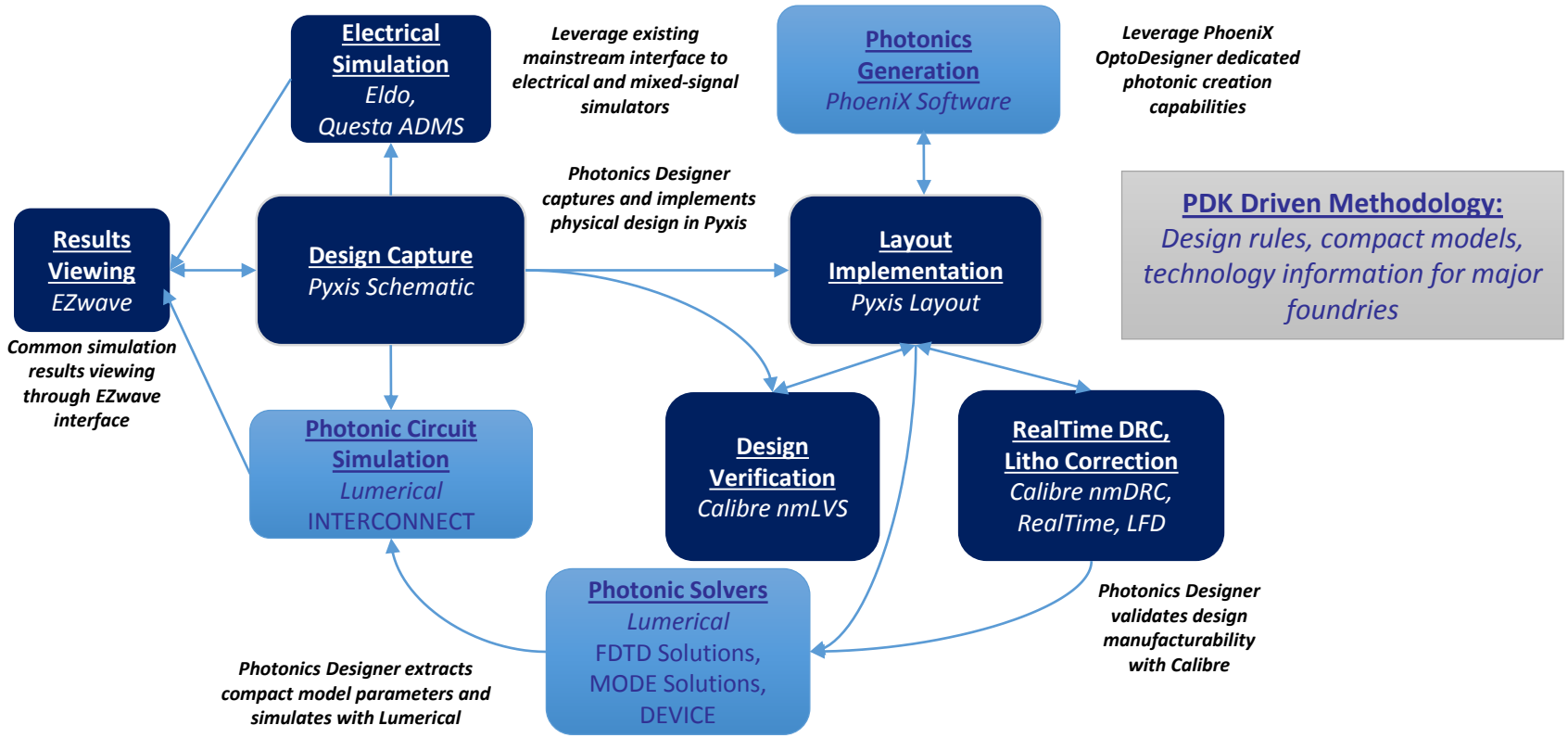



"Over the last three years, we've adopted Mentor and Lumerical tools to develop PDK- driven silicon photonics methodologies for our programs," said Professor Lukas Chrostowski, SiEPIC Program Director. "Lumerical provides excellent optical simulation tools, Mentor's Calibre provides best in class verification and Mentor's Pyxis provides the right framework for silicon photonics design. Our next workshop scheduled for October 24-28 includes a Pyxis PDK and fabrication with IME."

*A complete design flow for silicon photonics*

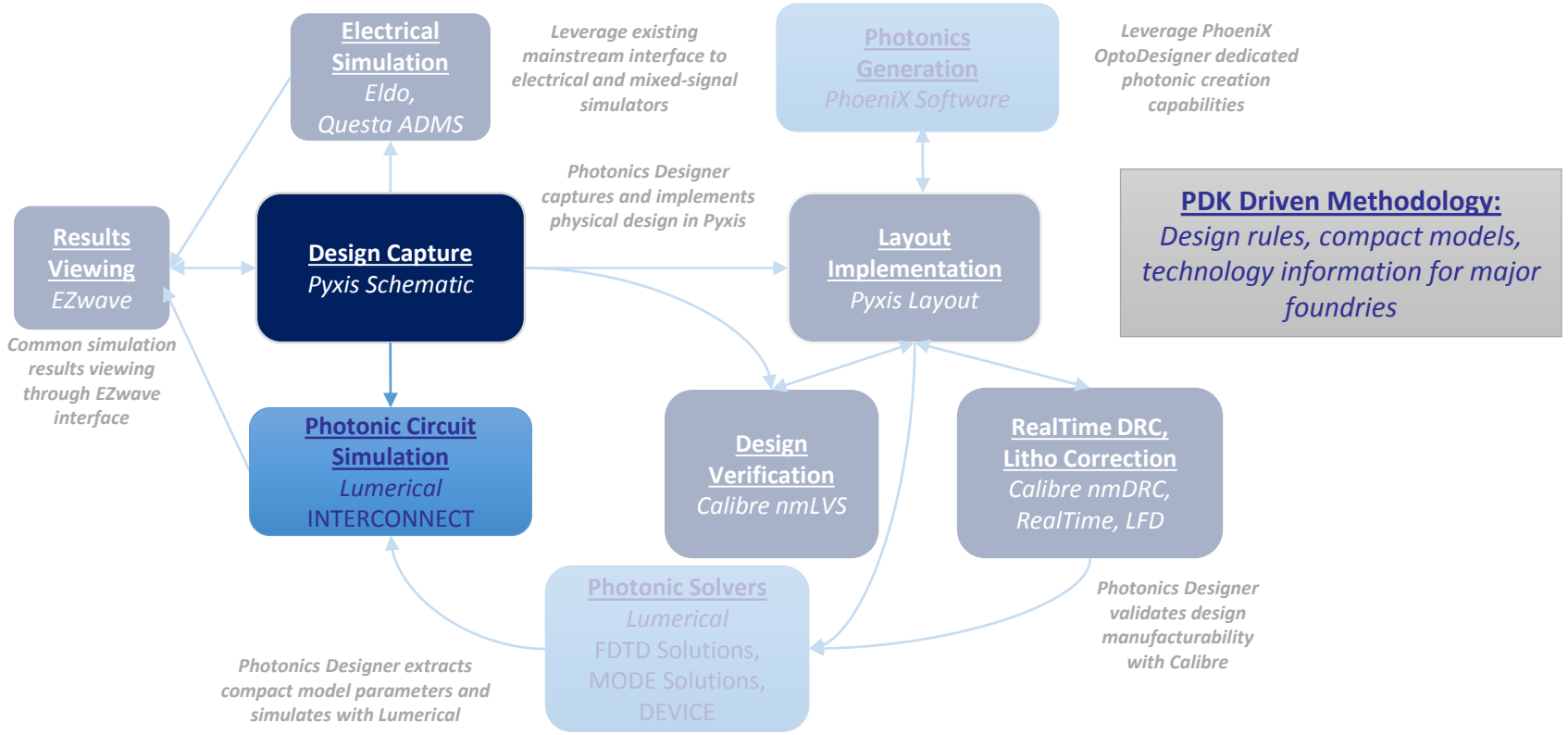
# *SILICON PHOTONICS FLOW INTRODUCTION*

# Design flow for silicon photonics




A generic, non-proprietary silicon photonics design kit is available for download at http://www.siepic.ubc.ca/GSiP

# Design flow for silicon photonics

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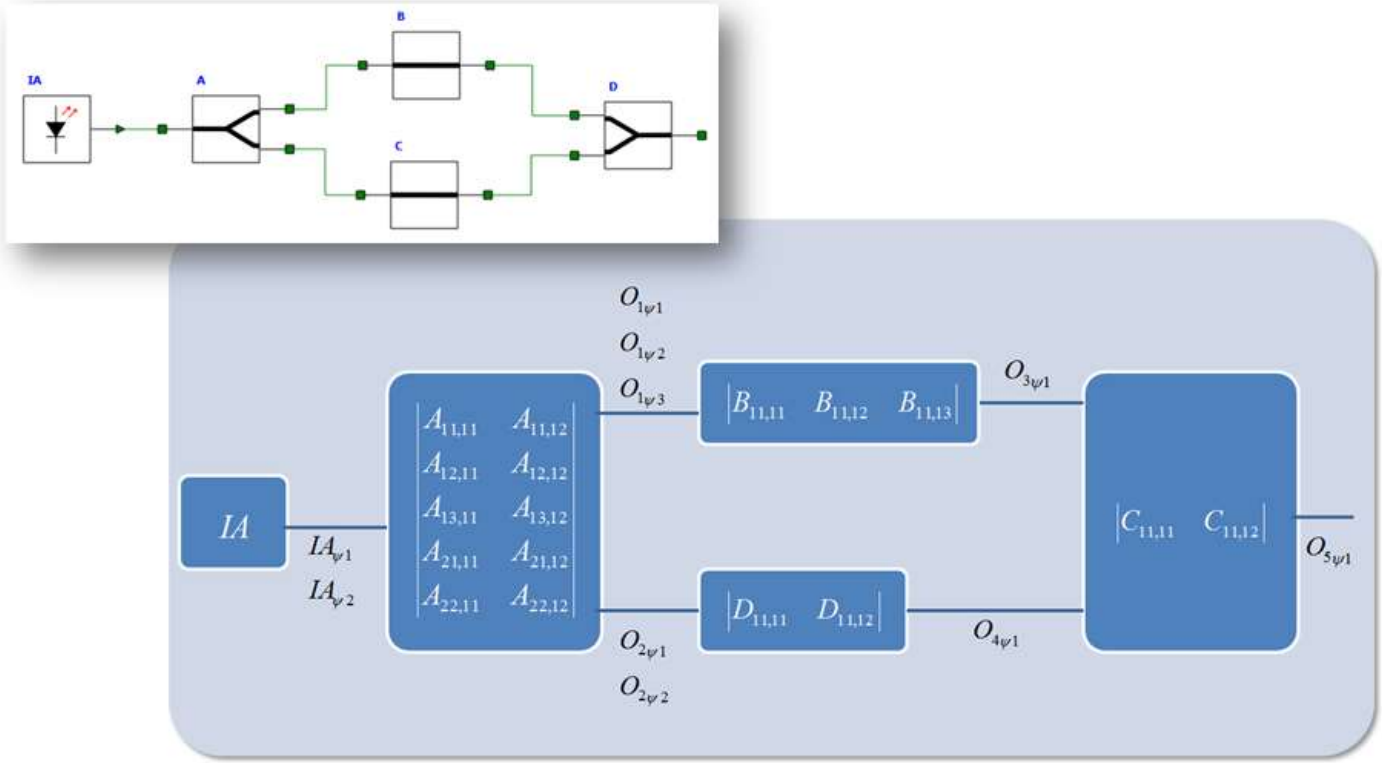
# *PHOTONIC IC CIRCUIT SIMULATION WITH INTERCONNECT*

# Photonic IC circuit simulation

- Frequency domain simulation: Scattering data analysis
  - ↗ Supports bidirectional, multimode and multichannel optical circuits



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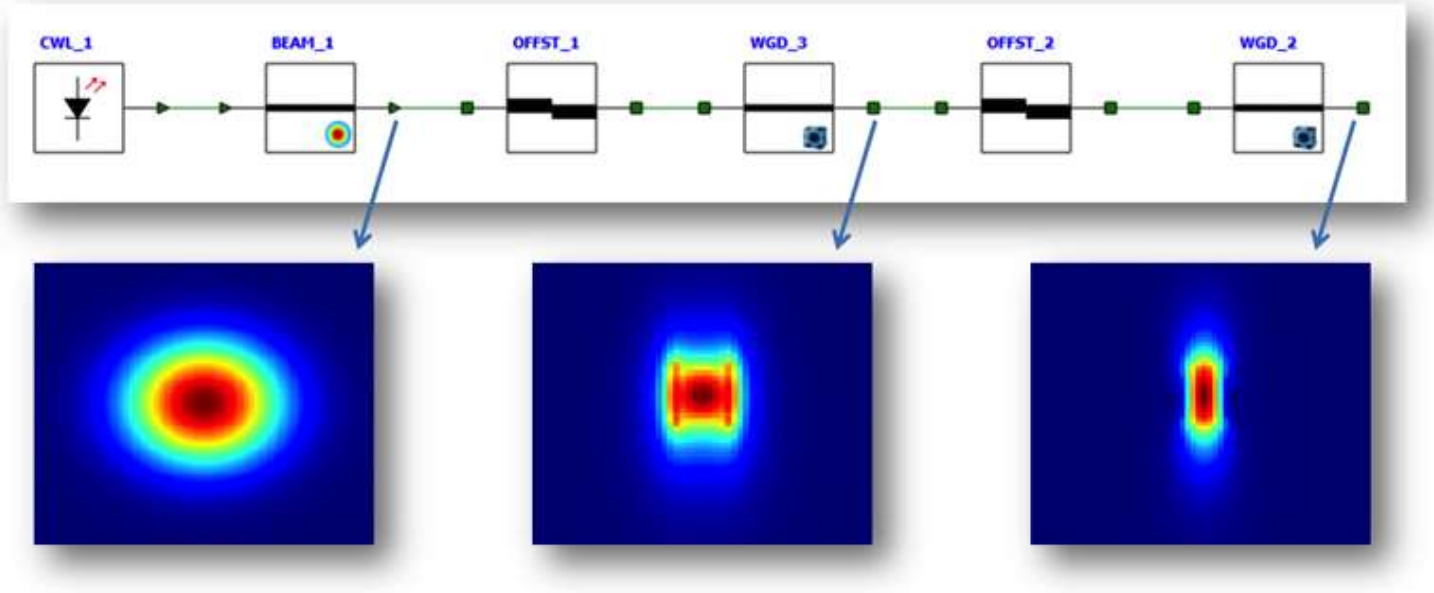

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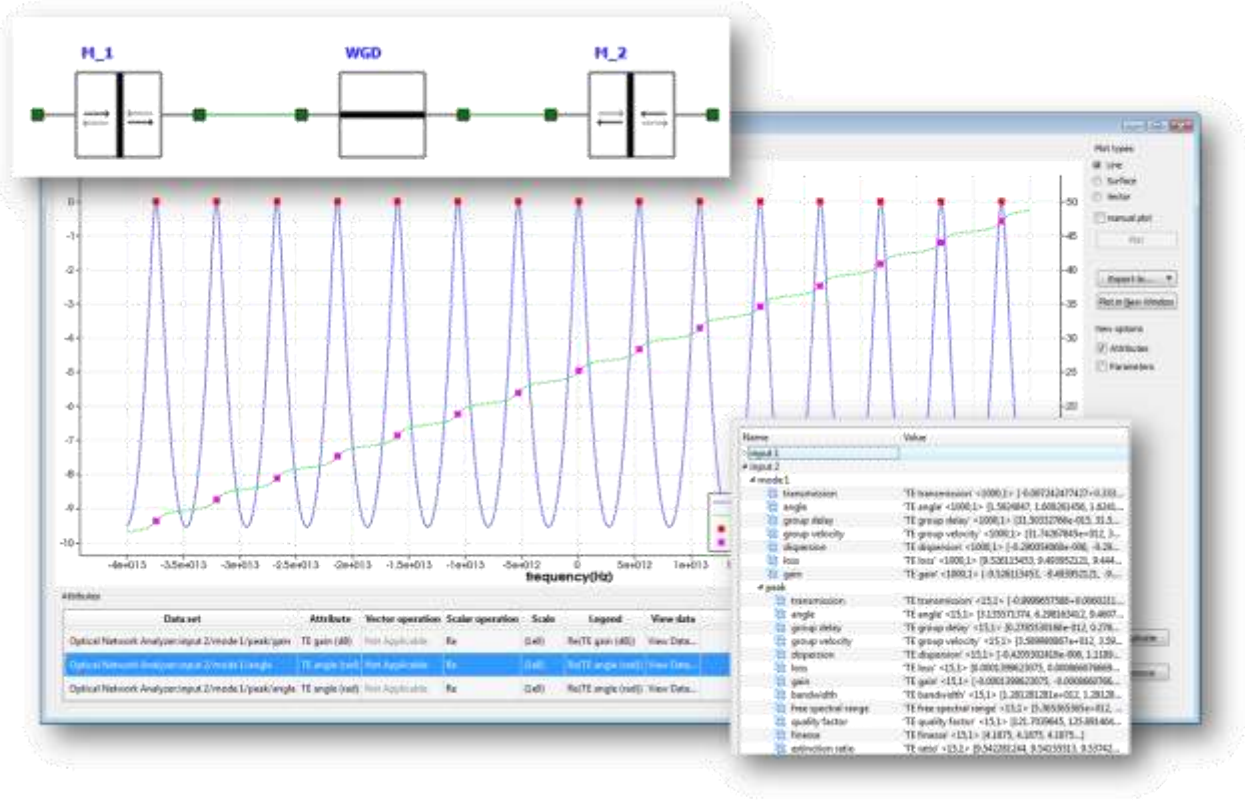

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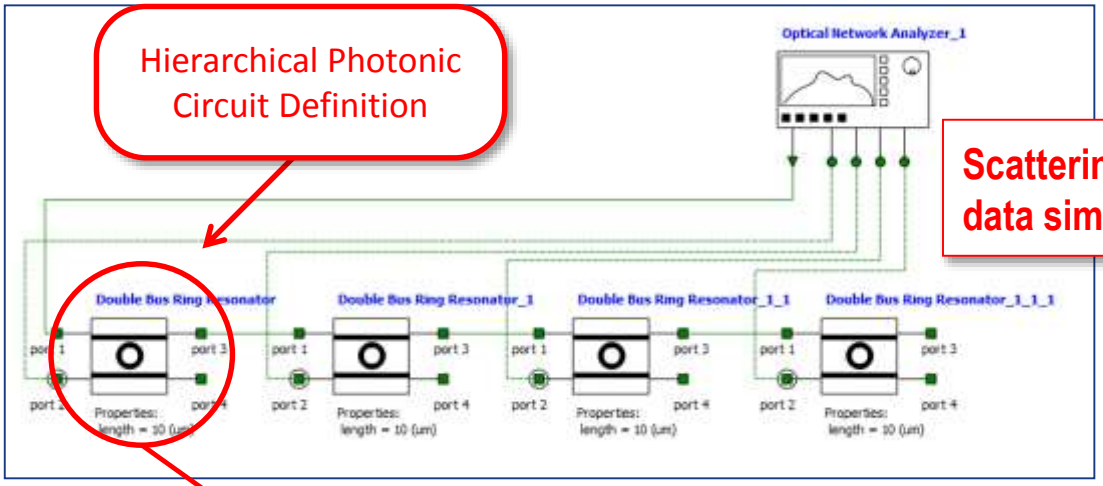
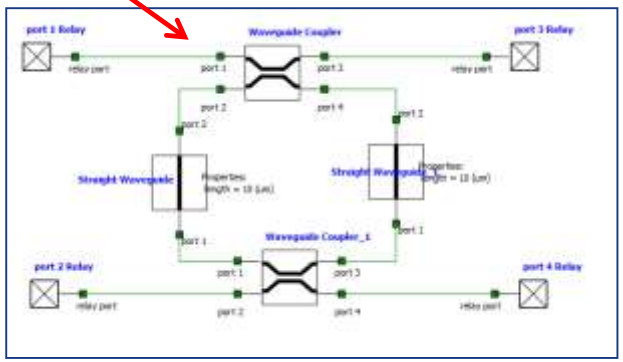
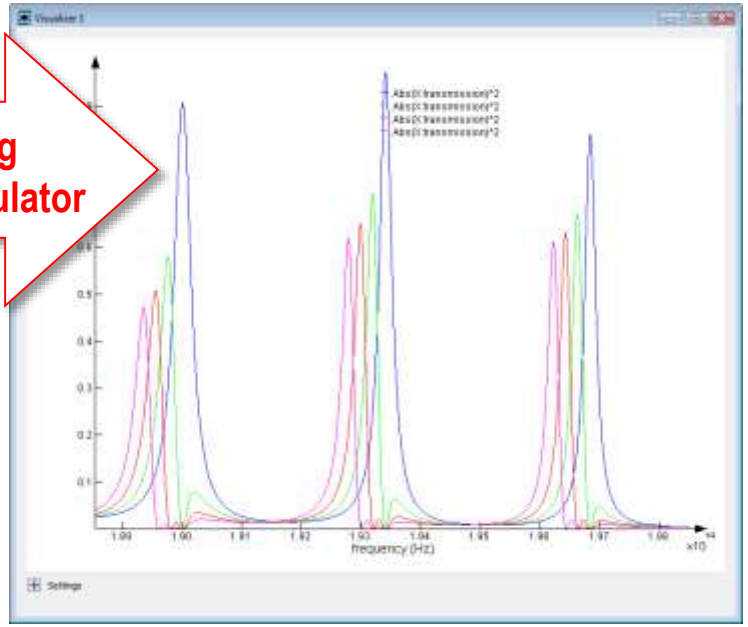


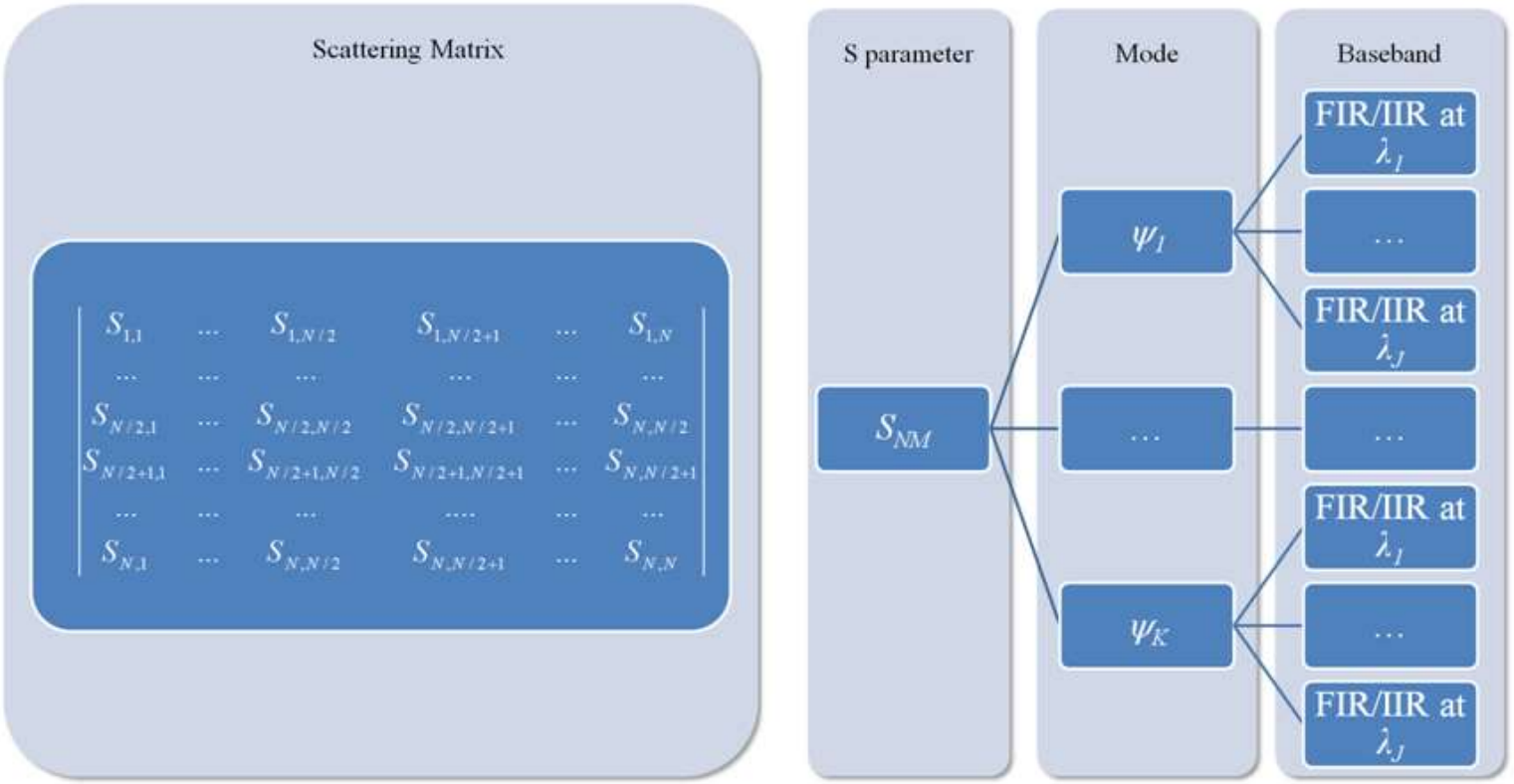




Scattering data simulator



# Photonic IC circuit simulation

- Time domain simulation: Transient analysis
  - ↗ Supports bidirectional, multimode and multichannel optical circuits



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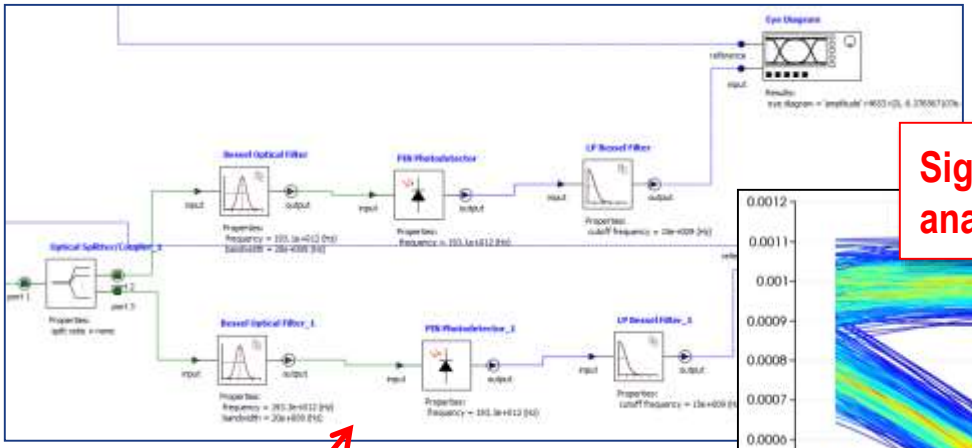
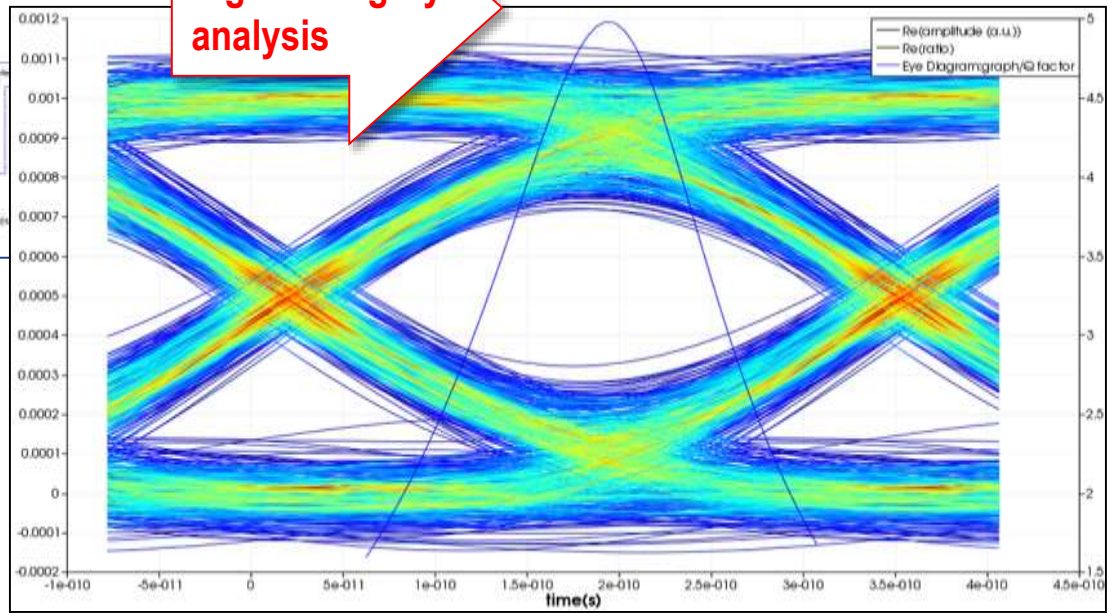


Mixed signal representation: digital, electrical and optical waveforms

Signal integrity analysis



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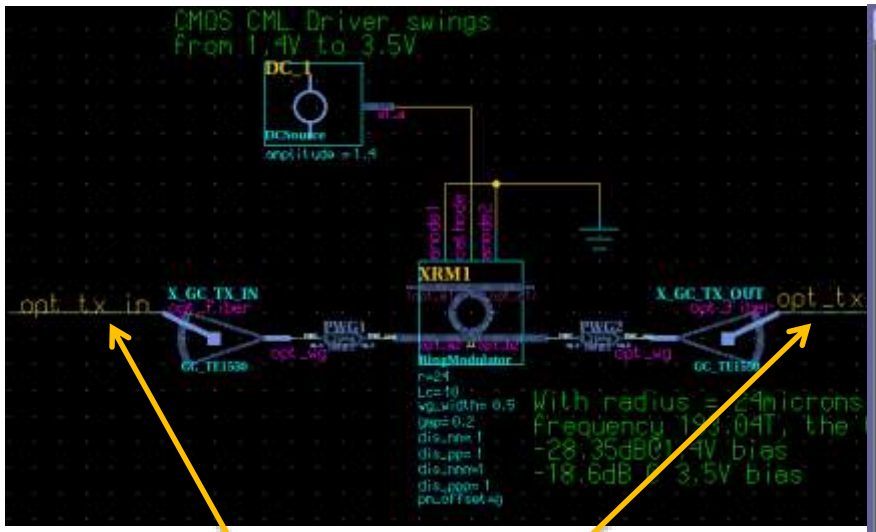
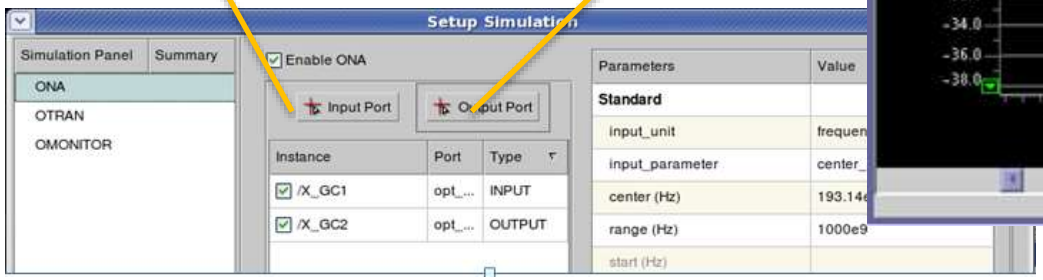
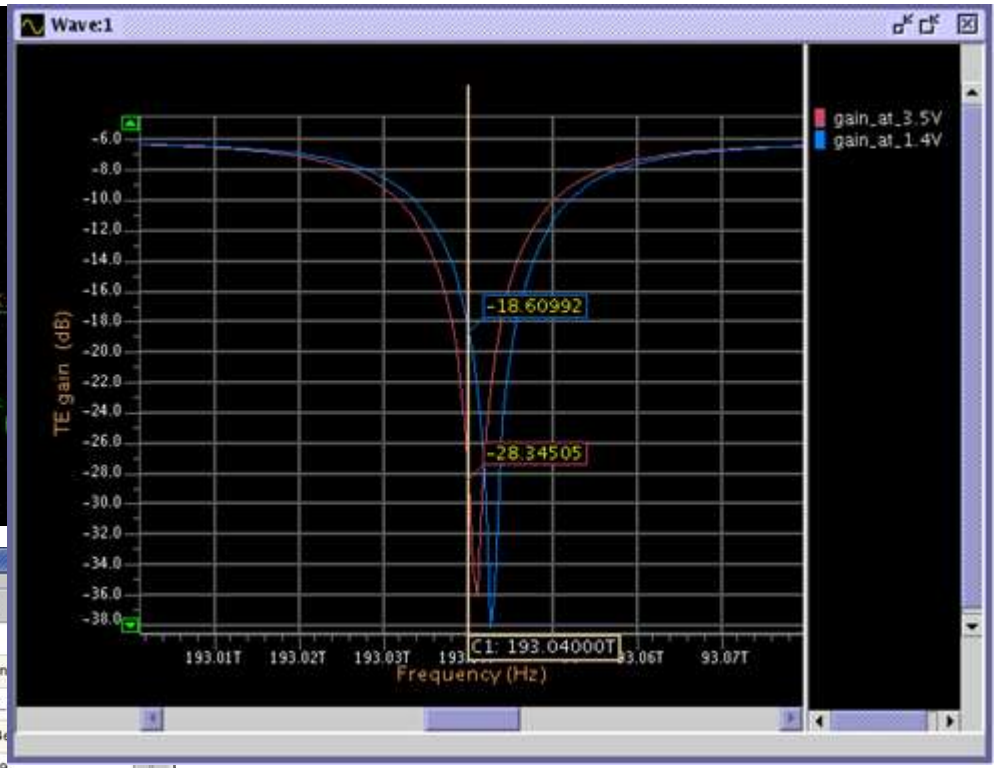
# *DRIVING INTERCONNECT FROM PYXIS*

# Driving INTERCONNECT from Pyxis

- Frequency domain spectral response
  - ↗ Interactively setup sizing and DC biasing of modulators in Pyxis with Lumerical INTERCONNECT ONA simulation
  - ↗ View results in Mentor's EZwave results viewer

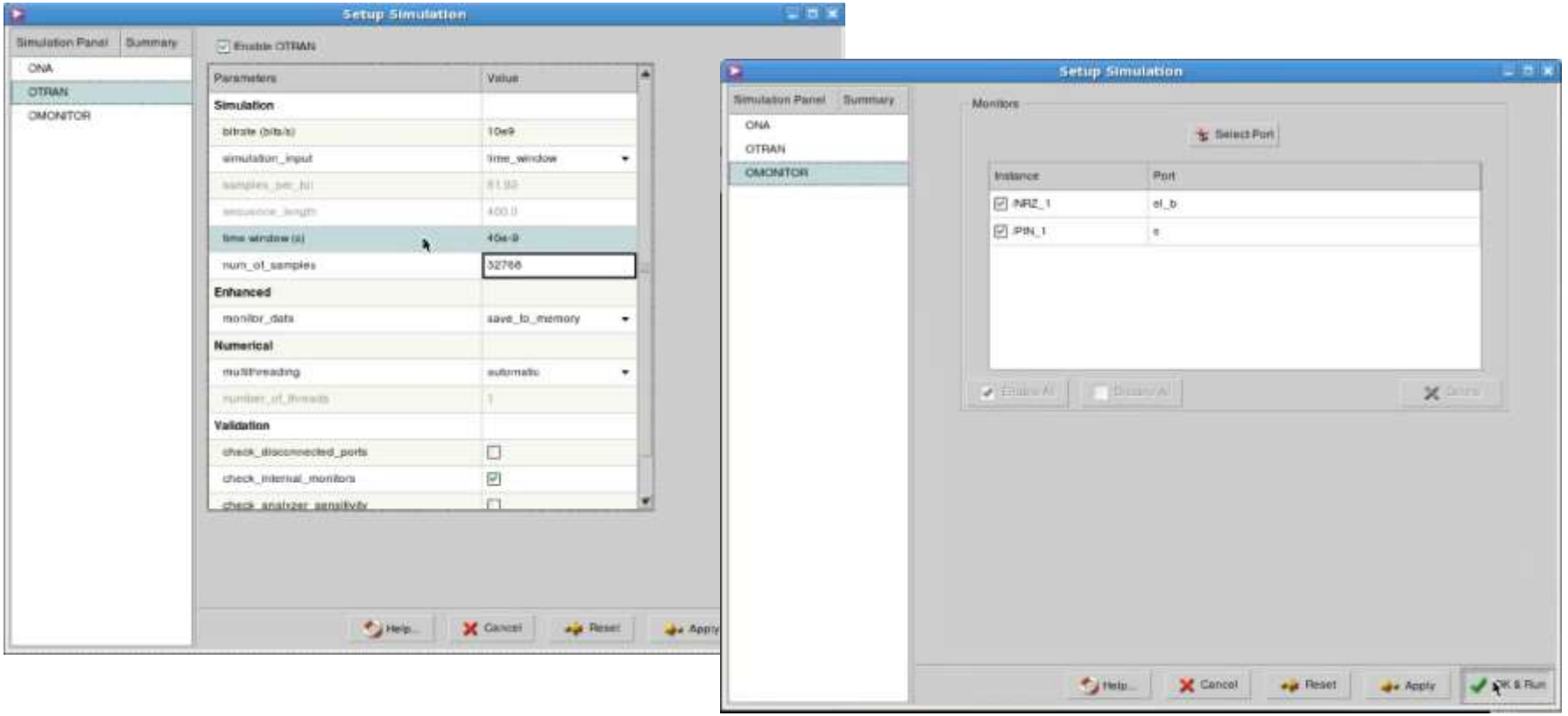


# Driving INTERCONNECT from Pyxis

- System level time domain simulation
  - ↗ User remains in Pyxis Schematic / EZwave cockpit for electrical and optical simulation

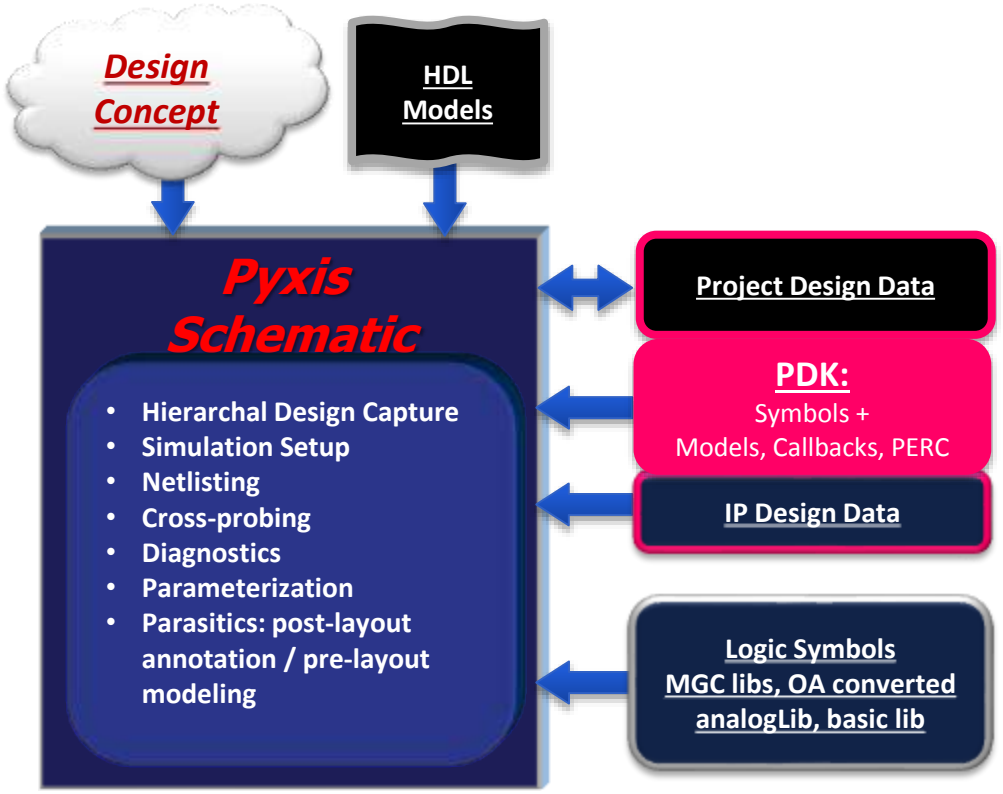


*A complete design flow for silicon photonics*

# *PDK DRIVEN FLOW WITH PYXIS AND CALIBRE*

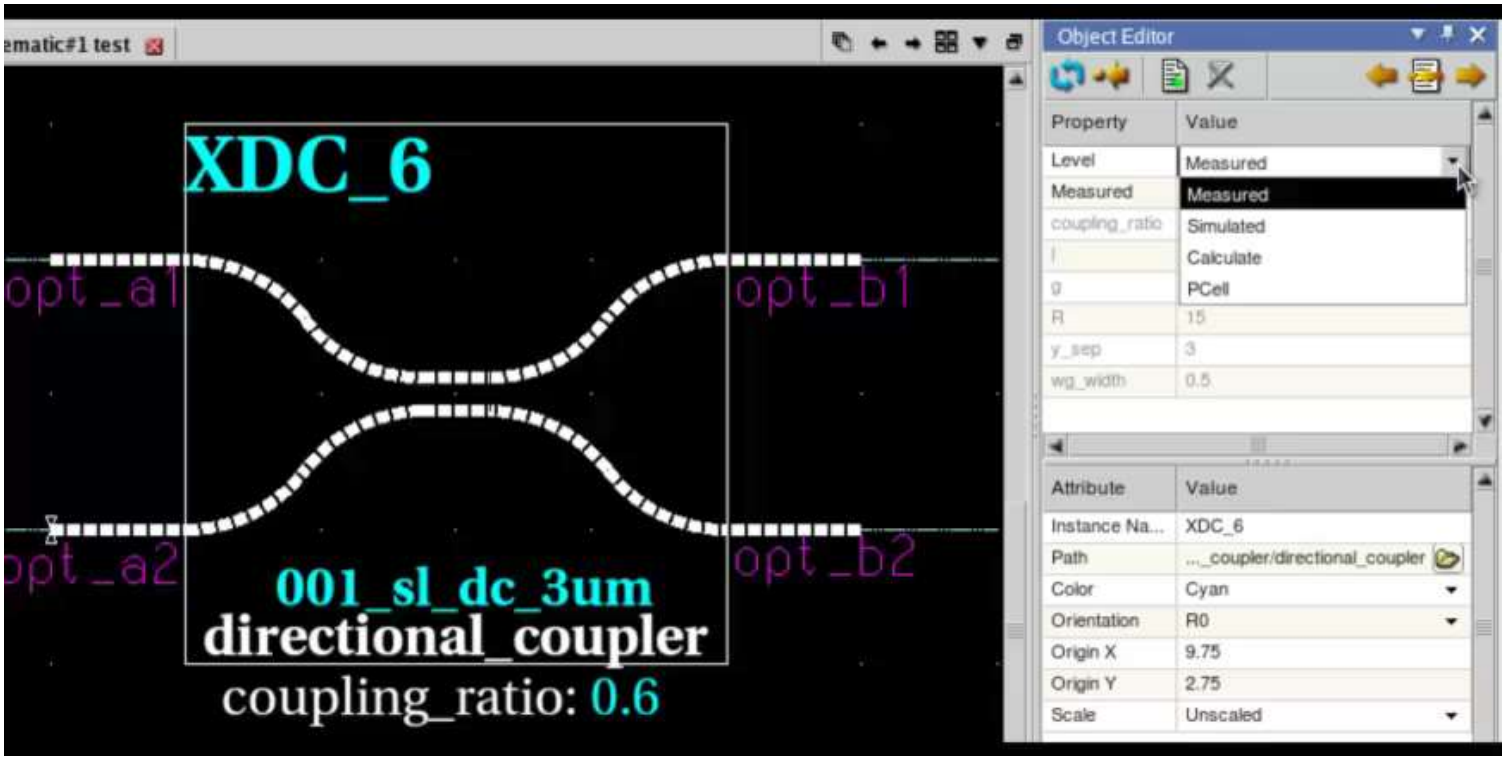
# *Design Creation/Capture*

- A complete environment to capture and simulate IC design concepts
- Supports Mixed Signal Language Modeling Formats
  - ↗ VHDL, Verilog, VHDL-AMS, Verilog-AMS
  - ↗ SPICE, VerilogA
- Integrated simulation flow supports fast iterations and analysis
- PDK driven to enable full design flow from schematic capture to post-layout simulation



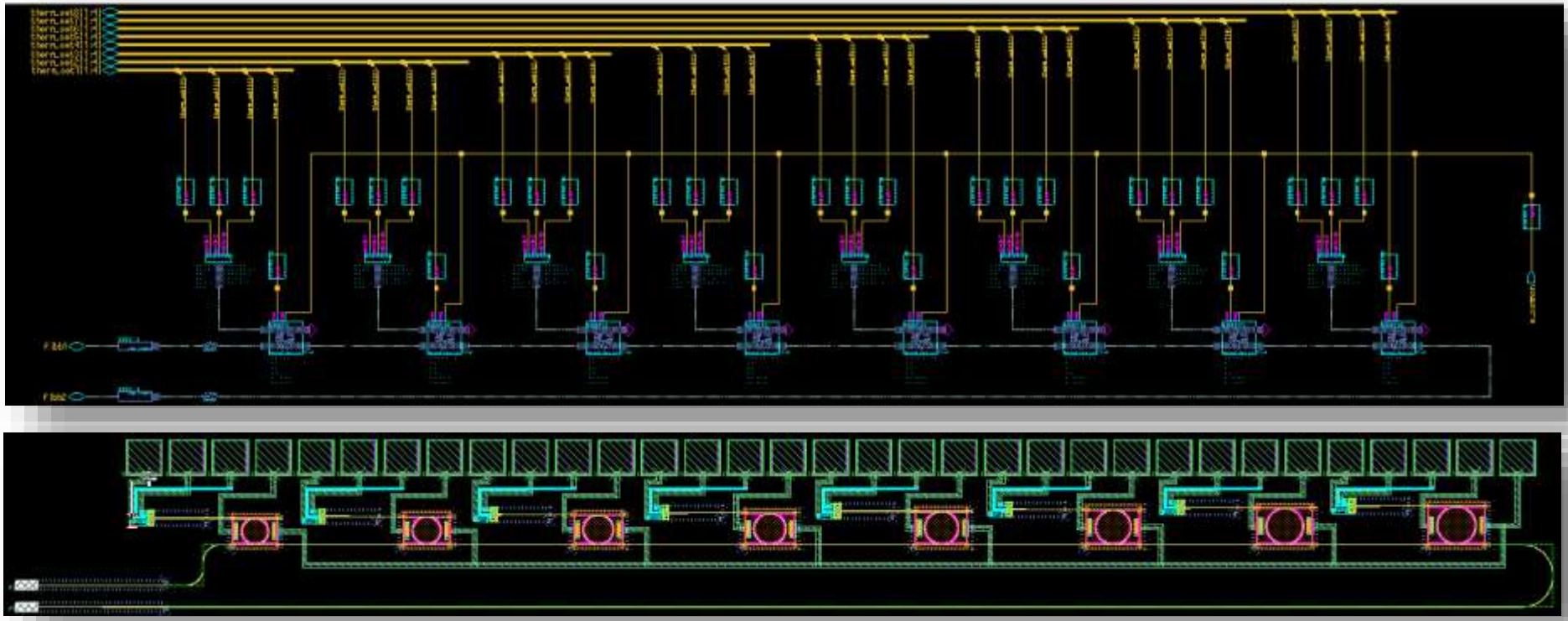
# Design Intent Based Property Editing

- Pyxis enables PDKs to be developed to assist to enter design parameters by system properties, not geometries
- Prototype Preview:



# *Silicon Photonics Schematic*
## *(with Actives)*

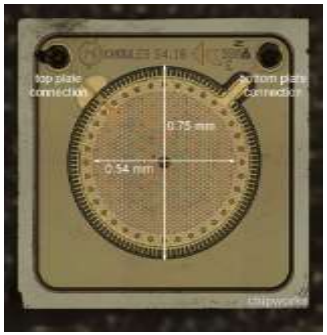
- Photonic and electrical connections automatically detected
- PDK supplied schematic checks for photonic connections
- Schematic connectivity drives layout directly

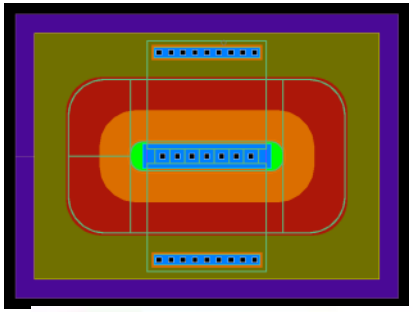


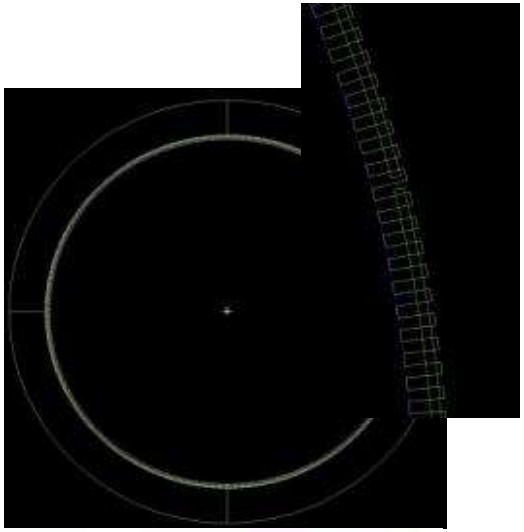
# Pyxis Framework Supports

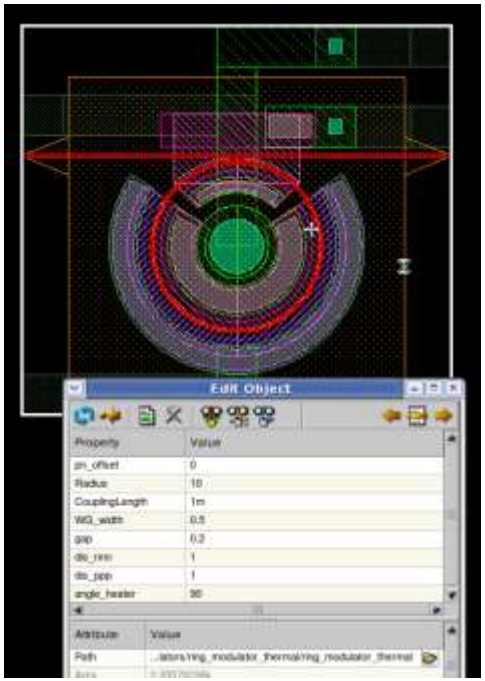
## All Angle Editing

- Pyxis Layout has been designed to support non-orthogonal layout
- Can add and rotate objects (paths, shapes, instances, devices) at any angle
- Current uses:
  - MEMs
  - TFT
  - Custom Power Devices
  - Silicon Photonics



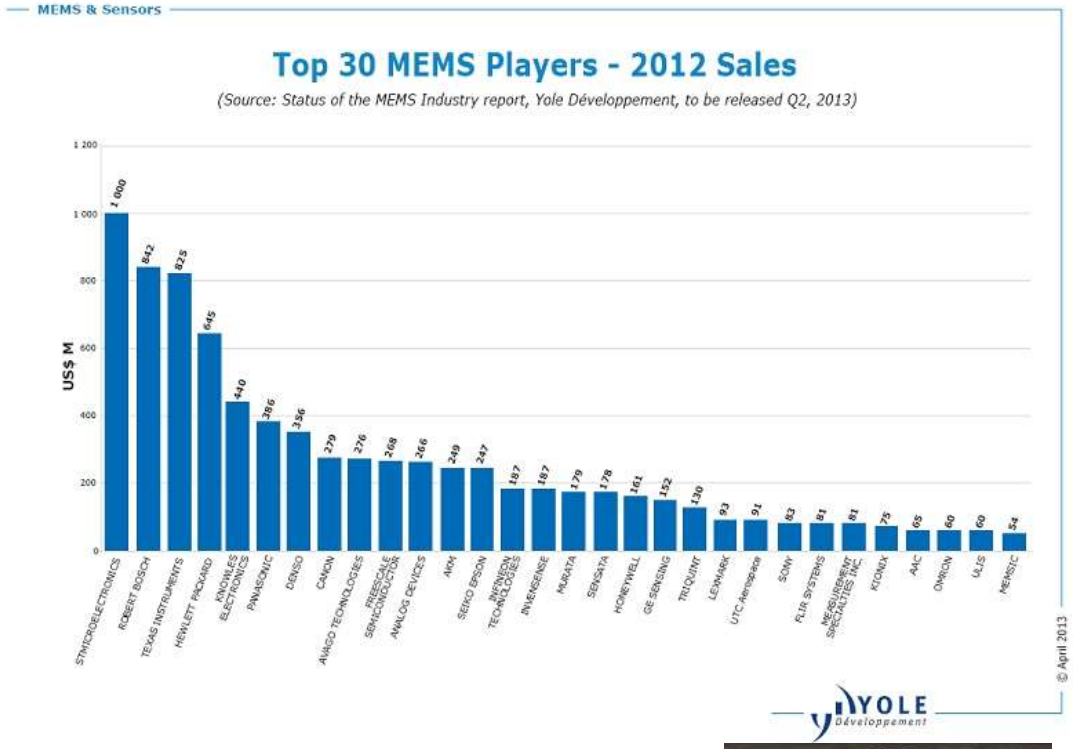





# MEMS Design Implementation

## *Pyxis Layout*

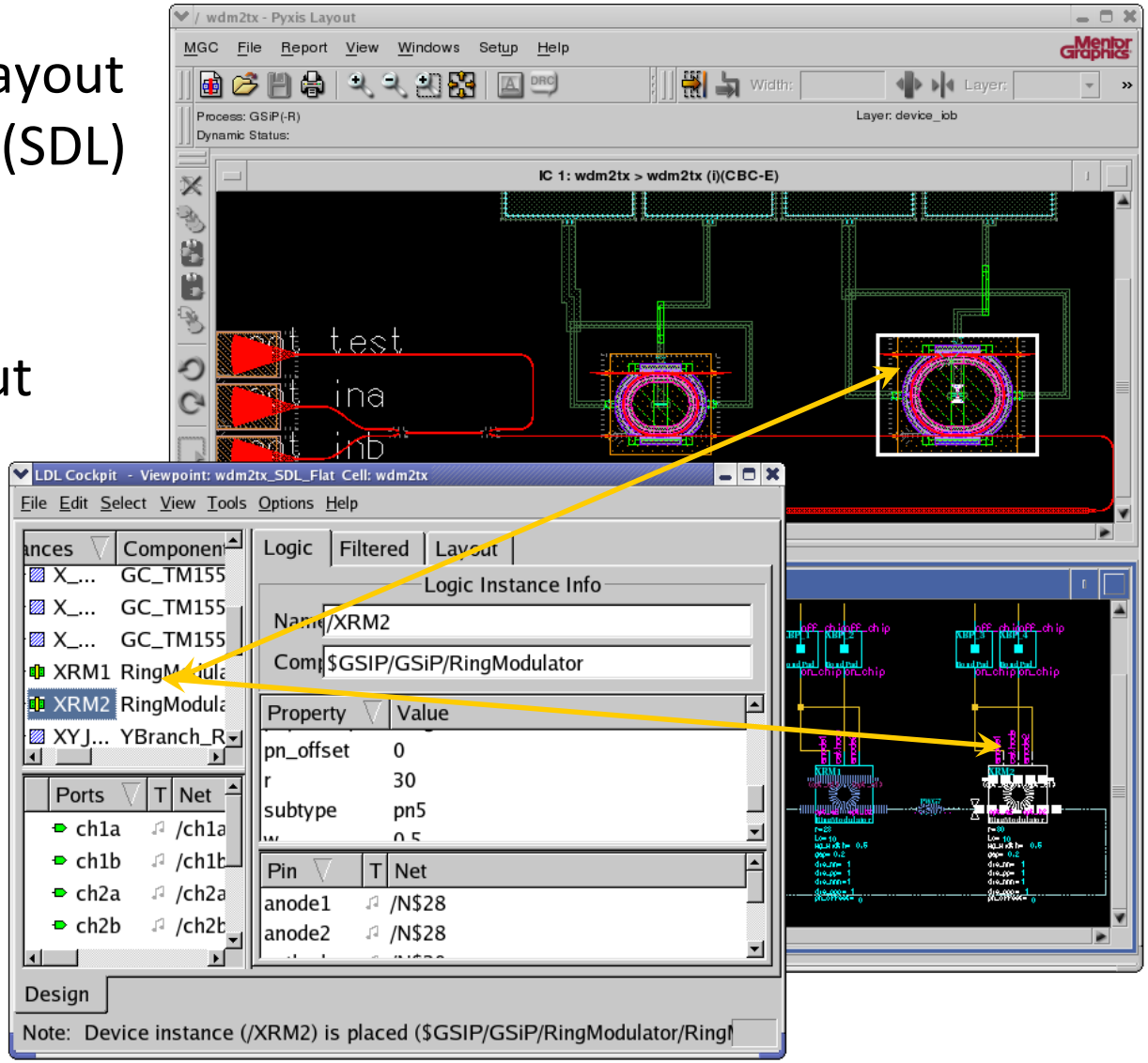
- Pyxis Layout used by five of the top ten suppliers
- Design types
  - ↗ Inkjets
  - ↗ Microphones
  - ↗ Accelerometers
  - ↗ Pressure sensor
- Leverages Pyxis Layout's unique capabilities in curvilinear applications






# Schematic/Connectivity Driven layout

- Connectivity-driven layout from both schematic (SDL) and netlist
- PCell support for fast foundry-correct layout
- Interactive connectivity driven routing for fast interconnect with waveguides or metal



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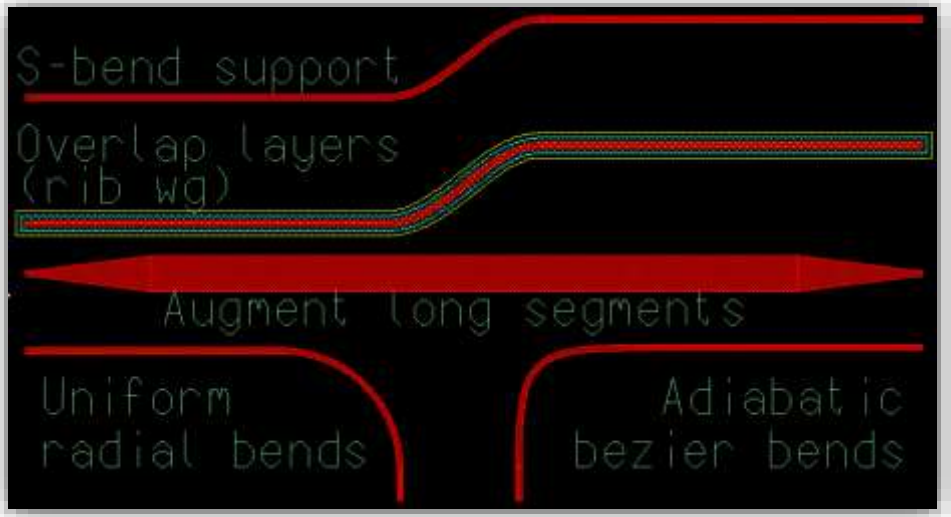
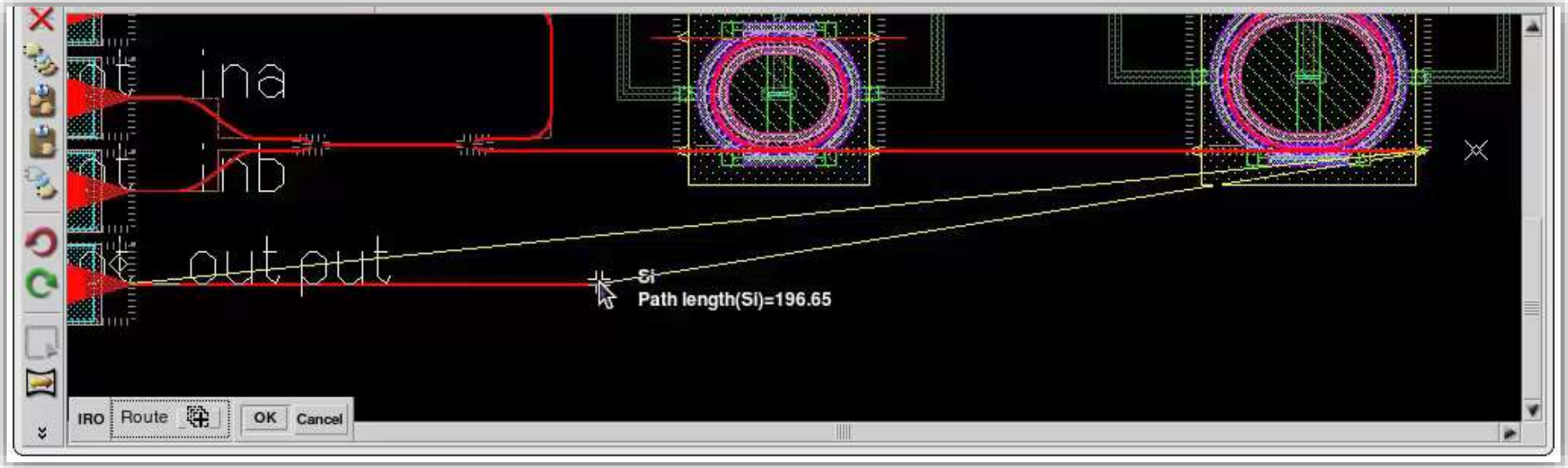



- Connectivity waveguide routing implemented using IRoute interactive router
- Supports overlap layers
- Keeps track of waveguide length and other key parameters for simulation



# Physical Verification for Silicon Photonics

## Calibre Verification Platform

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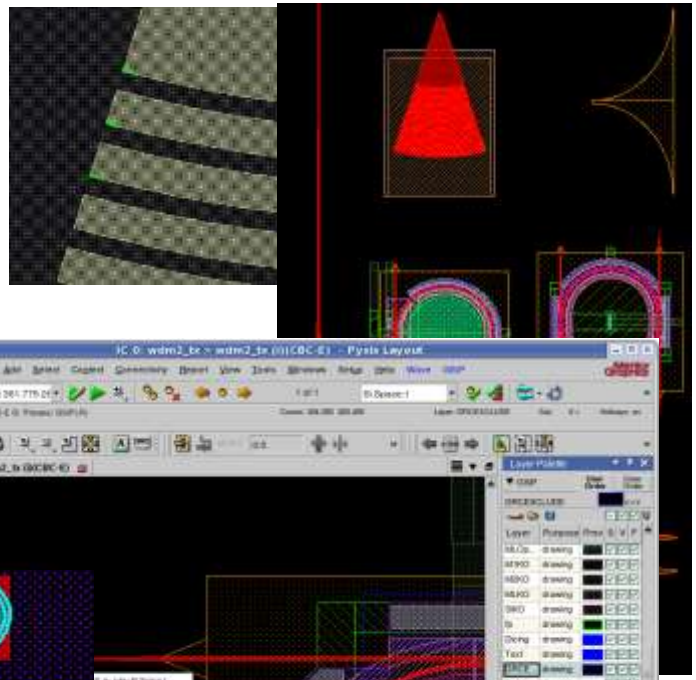
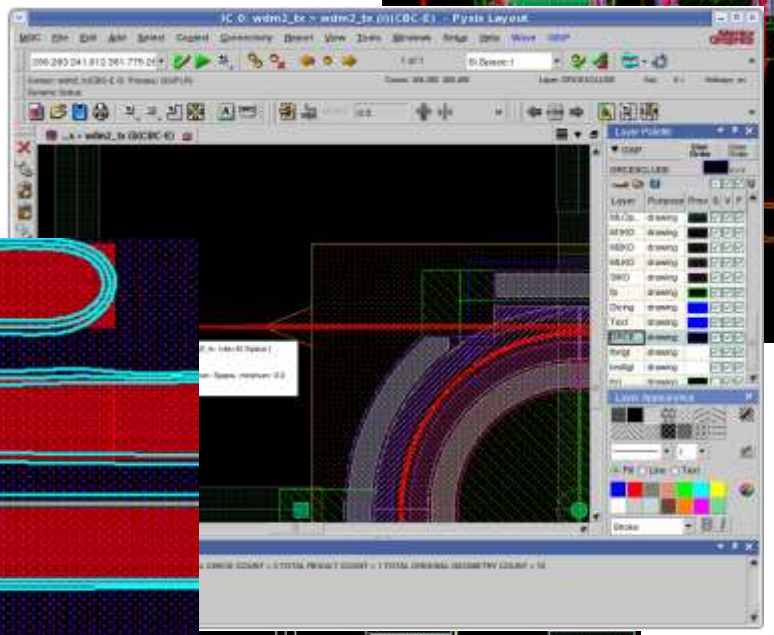
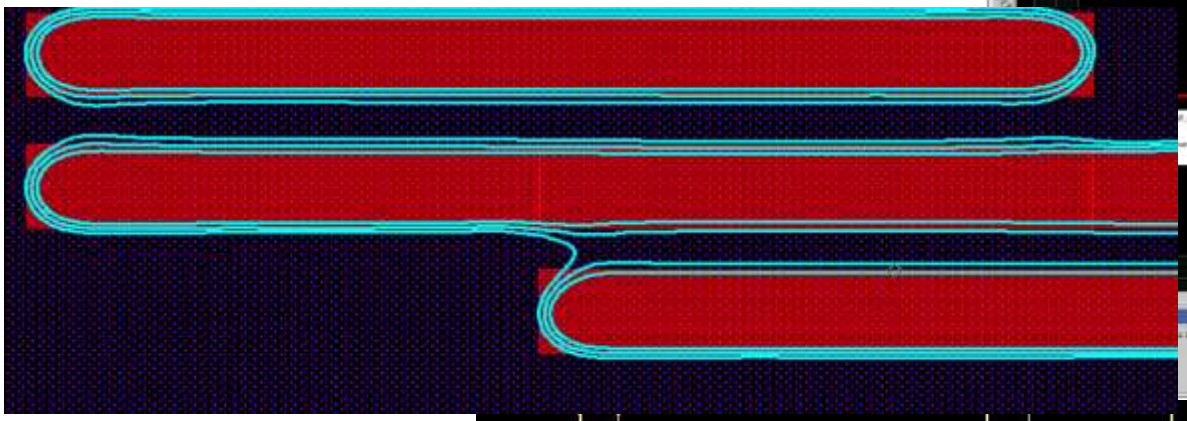
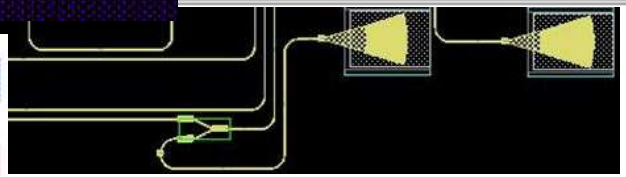
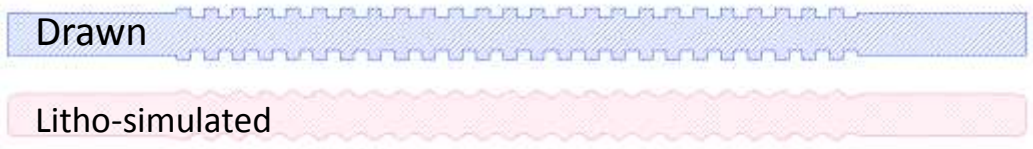
- Reducing “False” DRC Errors
- RealTime design integration
- Recognize & extract photonic devices
- Open detection & short isolation
- Wave guide curvature verification
- Lithographic Simulation





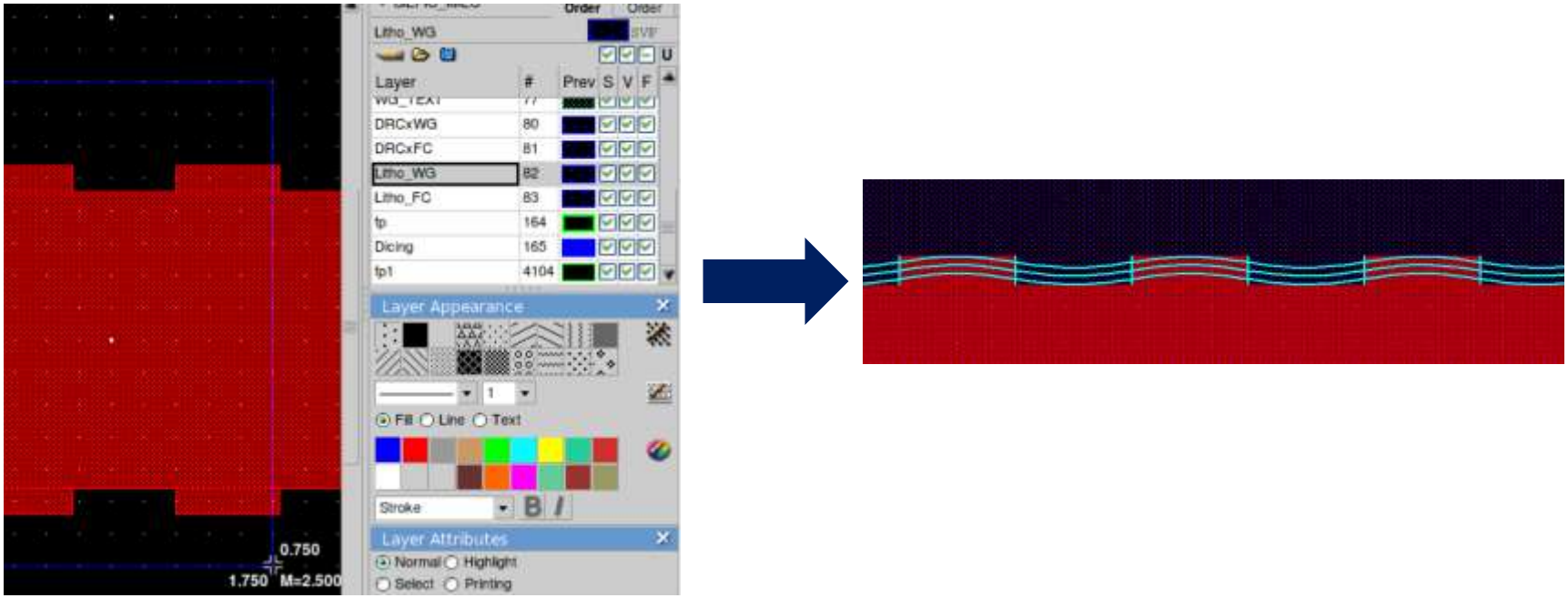






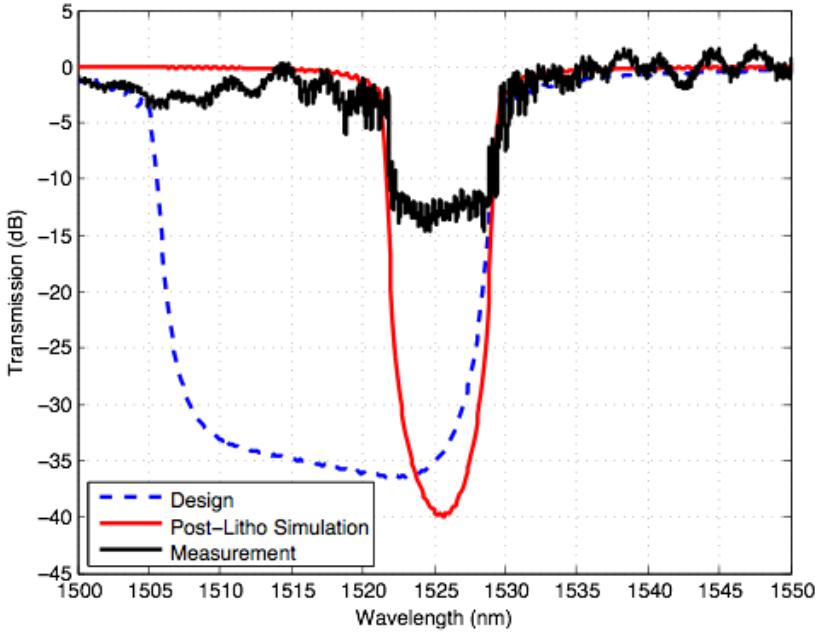
# Lithography Simulation

- Ideal sharp edges of grating will smooth due to lithography resolution
- This change in geometry will affect component attributes
- Run a Calibre LFD lithography simulation directly in Pyxis Layout window with Calibre RealTime or on exported GDS/Oasis data

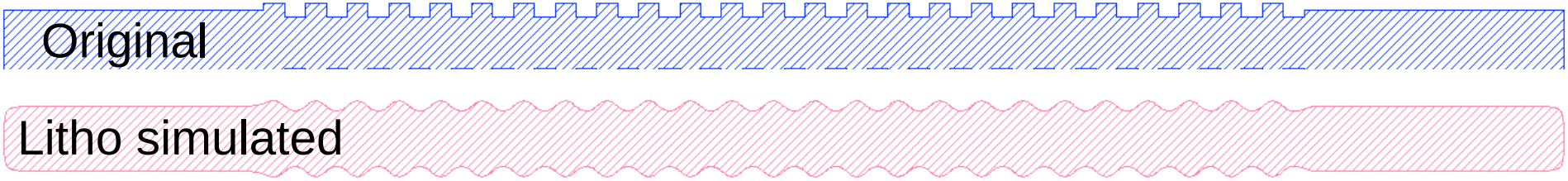


# *Simulation of Lithography Effects*

- Comparison of device designed with 40 nm square corrugations
- Litho Correction and FDTD Solutions simulations match experimental Bragg bandwidth

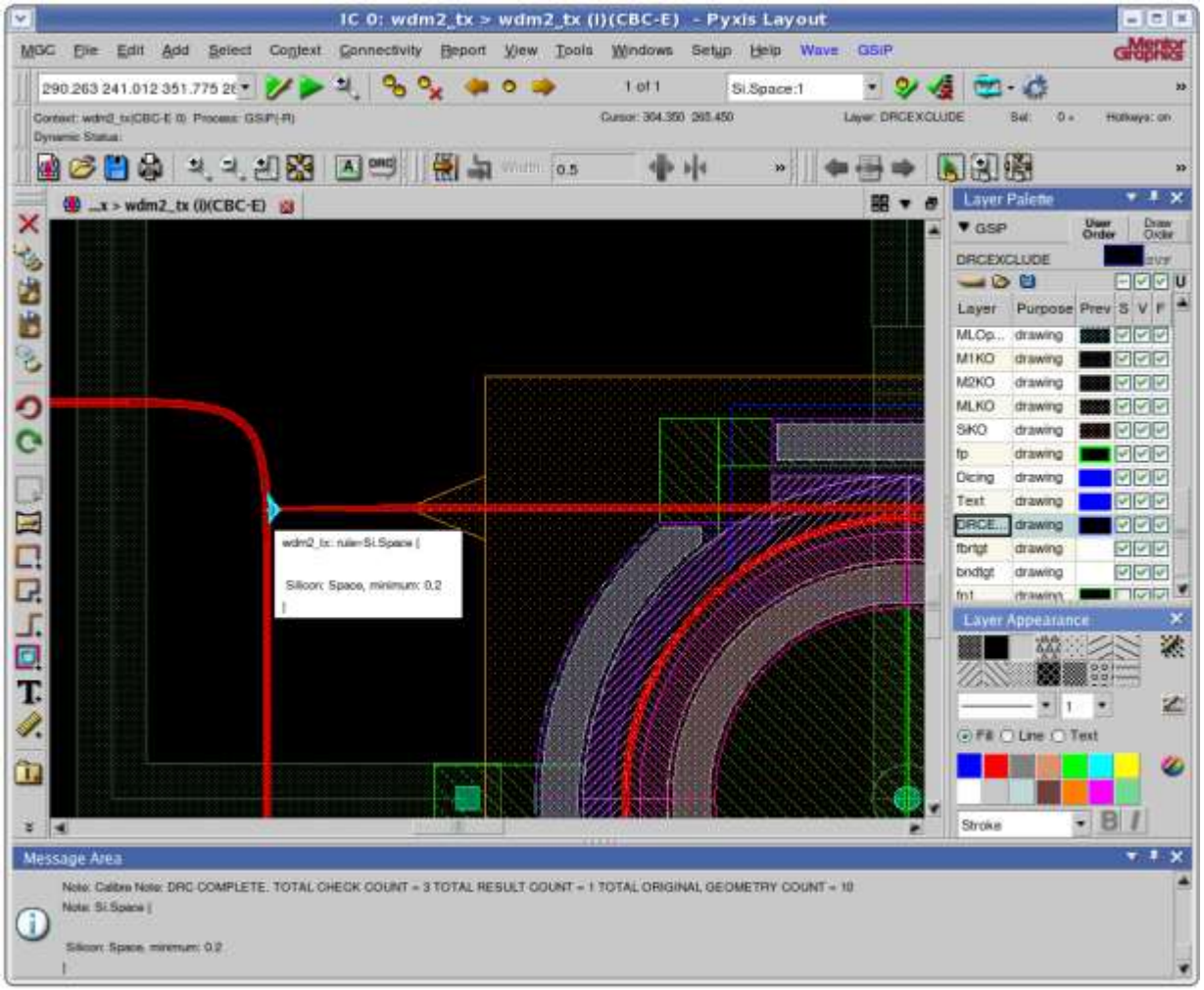



Xu Wang, et al., "**Lithography Simulation for the Fabrication of Silicon Photonic Devices with Deep-Ultraviolet Lithography**", *IEEE GFP,* 2012



# Calibre RealTime Interface

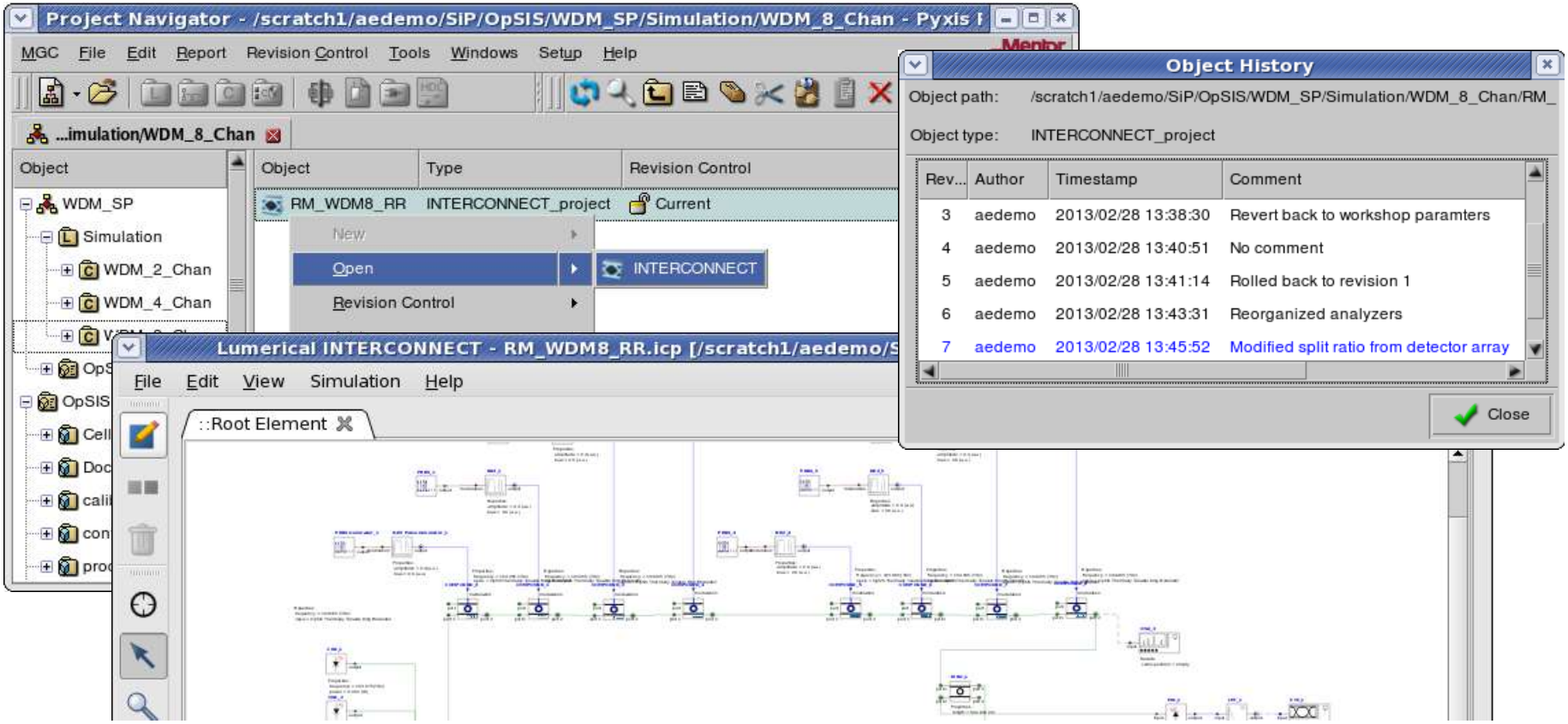
- Sign-off quality DRC as you edit, using standard Calibre decks
- Setup and Manage DRC Checking Recipes
- Navigate and fix errors in the design tool
- Supports Calibre Interactive LVS, DRC, xRC/ xACT and PERC




**Real-time signoff DRC means better layout in less time**

# The Pyxis Framework

## Data Management with Revision Control

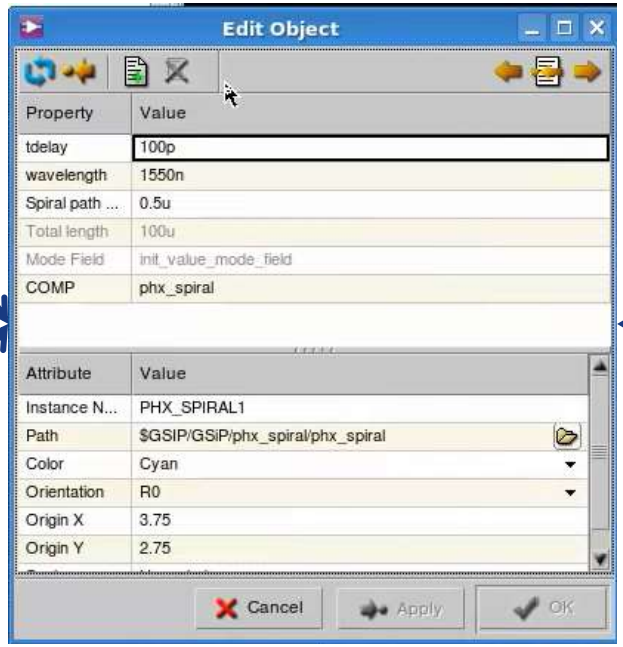



- Pyxis Project Manager can easily manage 3rd party data and tool invocation with ClioSoft SOS EDA style revision control

# Enhancing Methodology

## PhoeniX Collaboration

- Using CMS Call backs for D.I.B. property editing
  - ↗ Designer enters time delay, width and desired wavelength
  - ↗ PhoeniX returns implementation parameters to schematic and layout
  - ↗ PhoeniX creates PCell enabling full Schematic Driven Layout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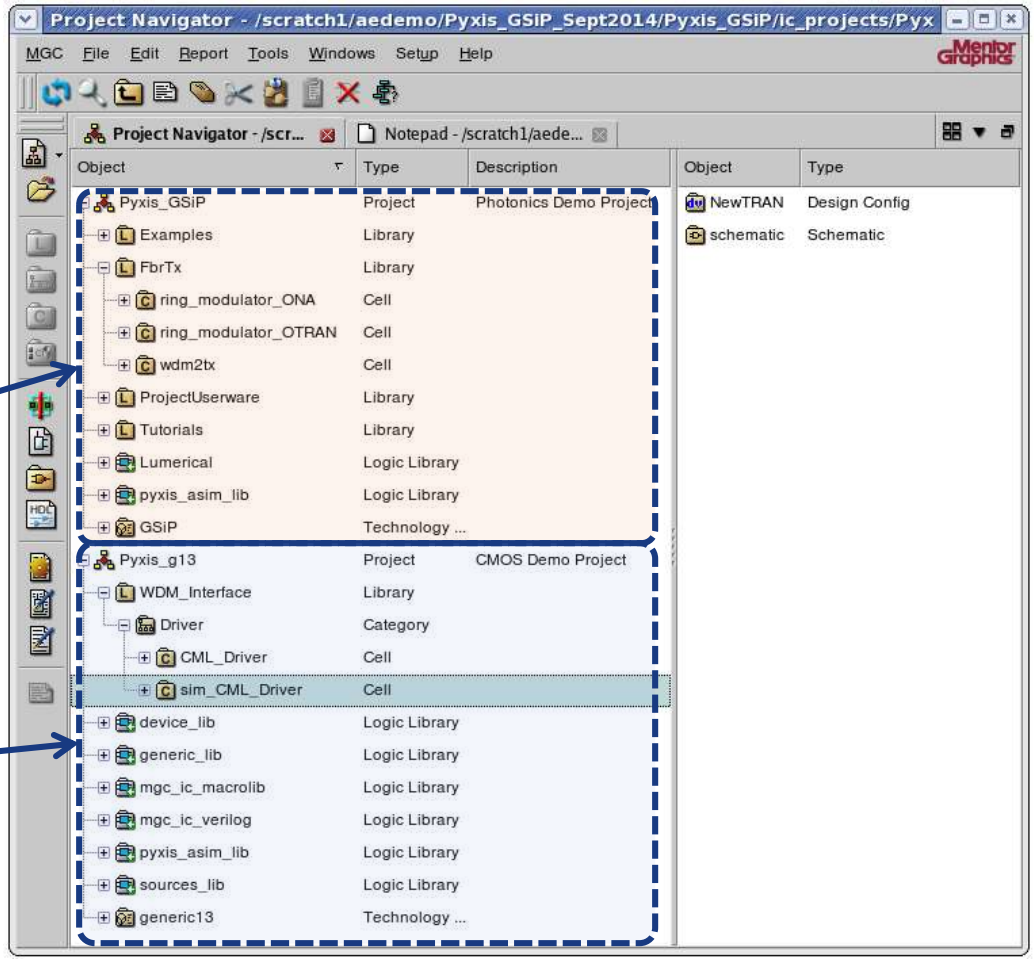
# *PHOTONICS + CMOS*

# Photonics + CMOS

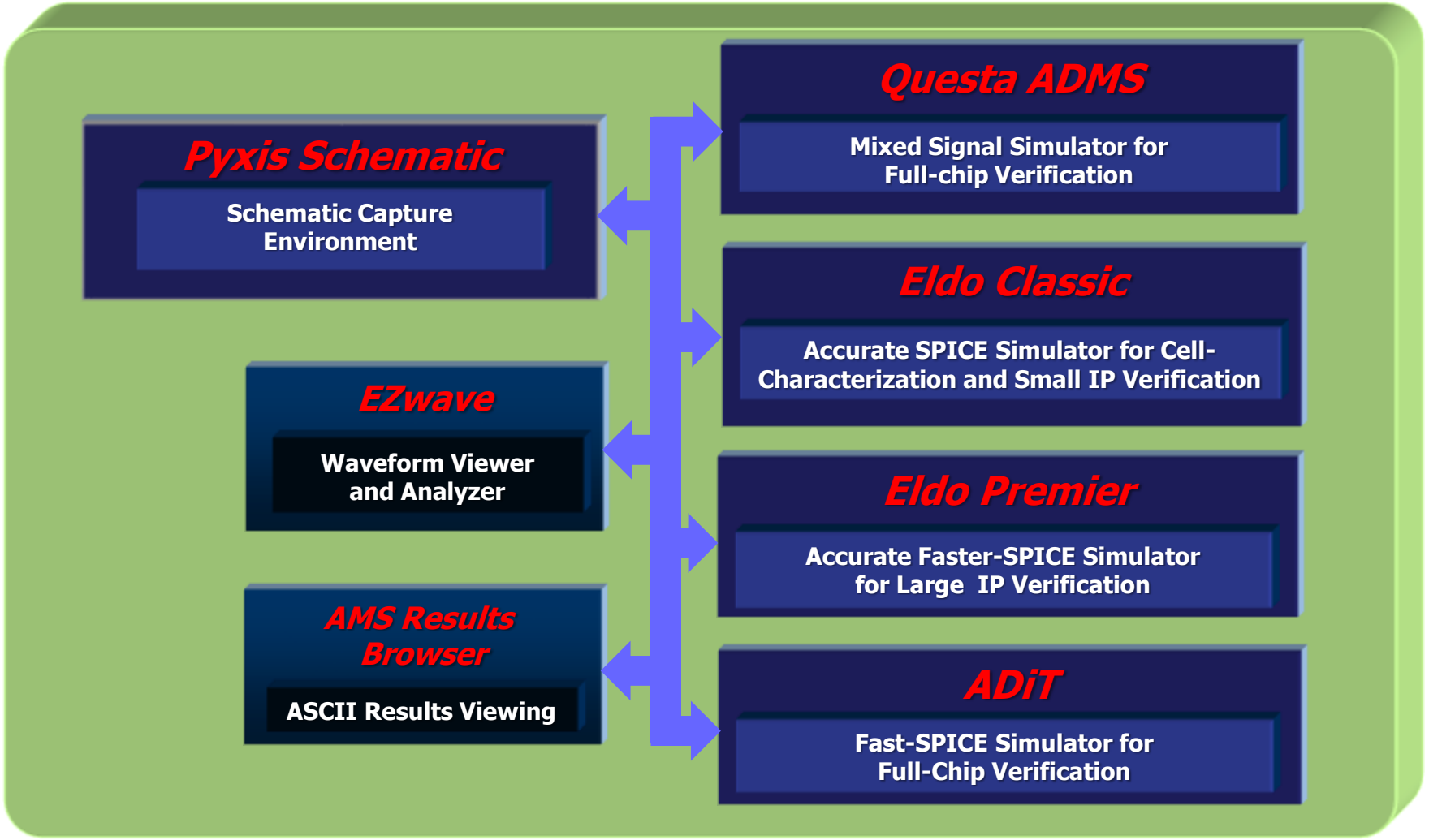
## Common data management environment

- Pyxis Project Manager enables multi-project viewing
- Silicon Photonics design project
  - ↗ GSiP PDK
- CMOS design project
  - ↗ generic13 PDK



# Photonics + CMOS

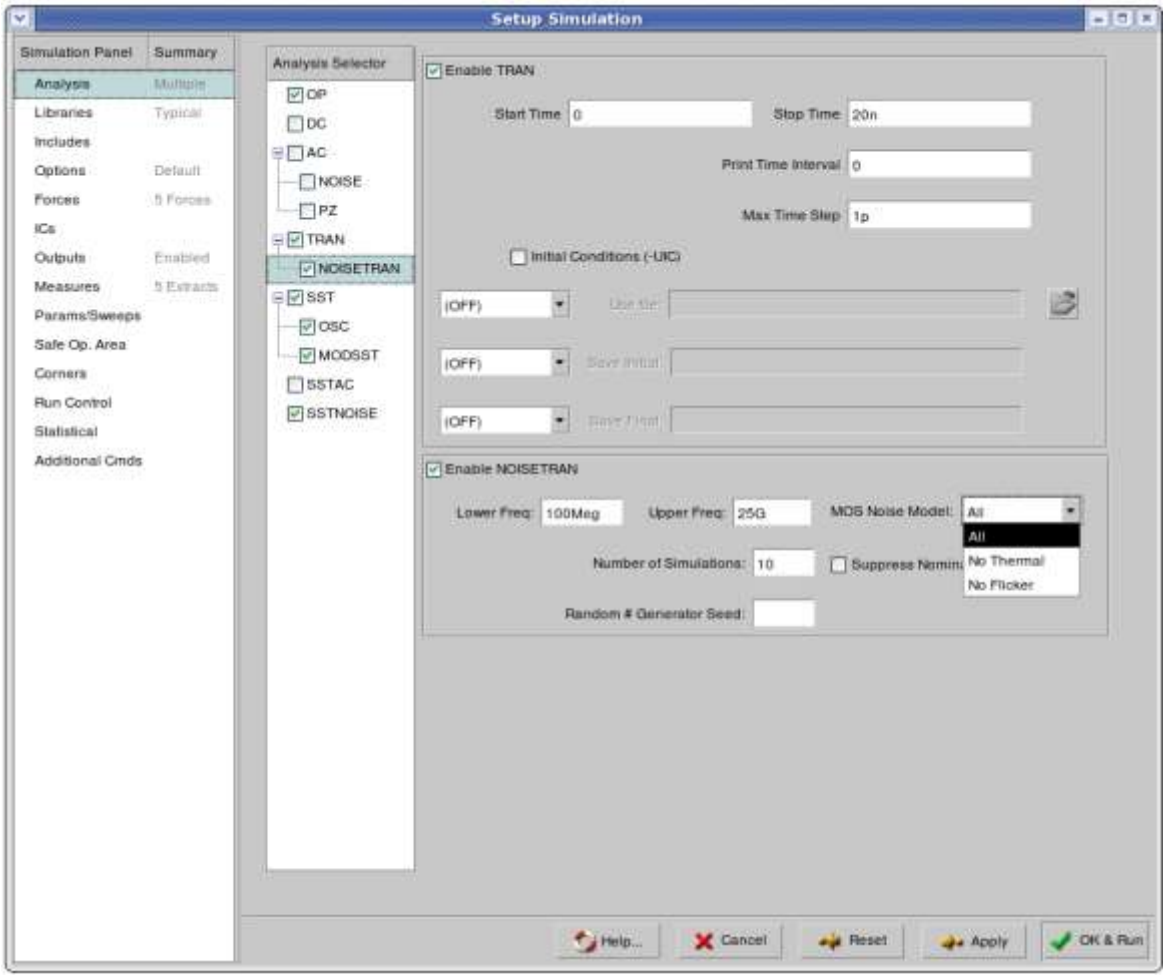
## Pyxis integration to AMS products



# Photonics + CMOS

## Comprehensive simulation setup

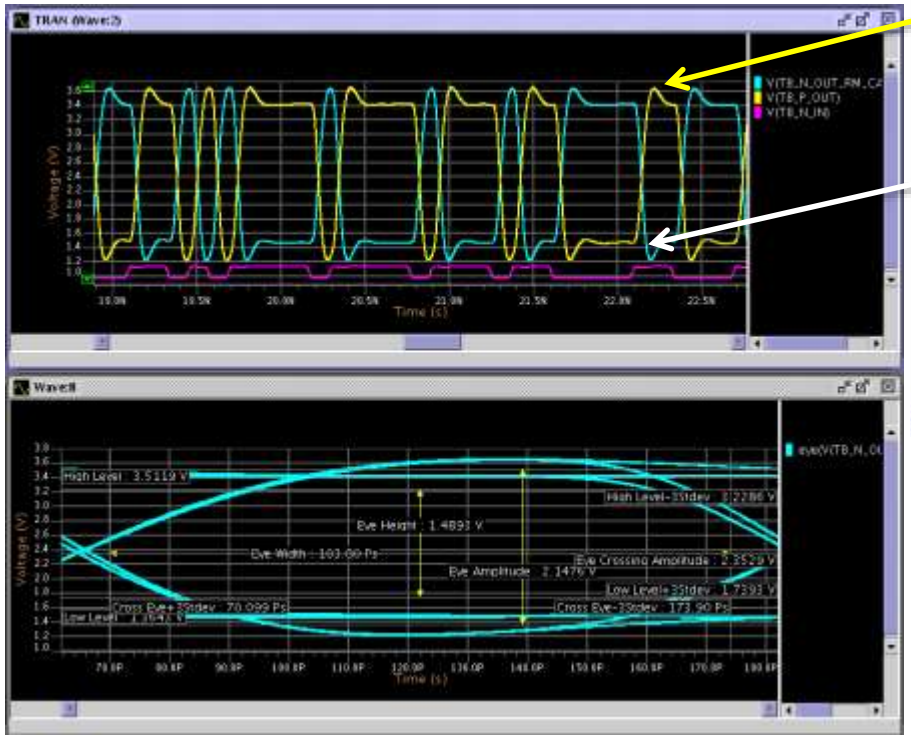
- Setup and configure simulation analyses available with the simulator

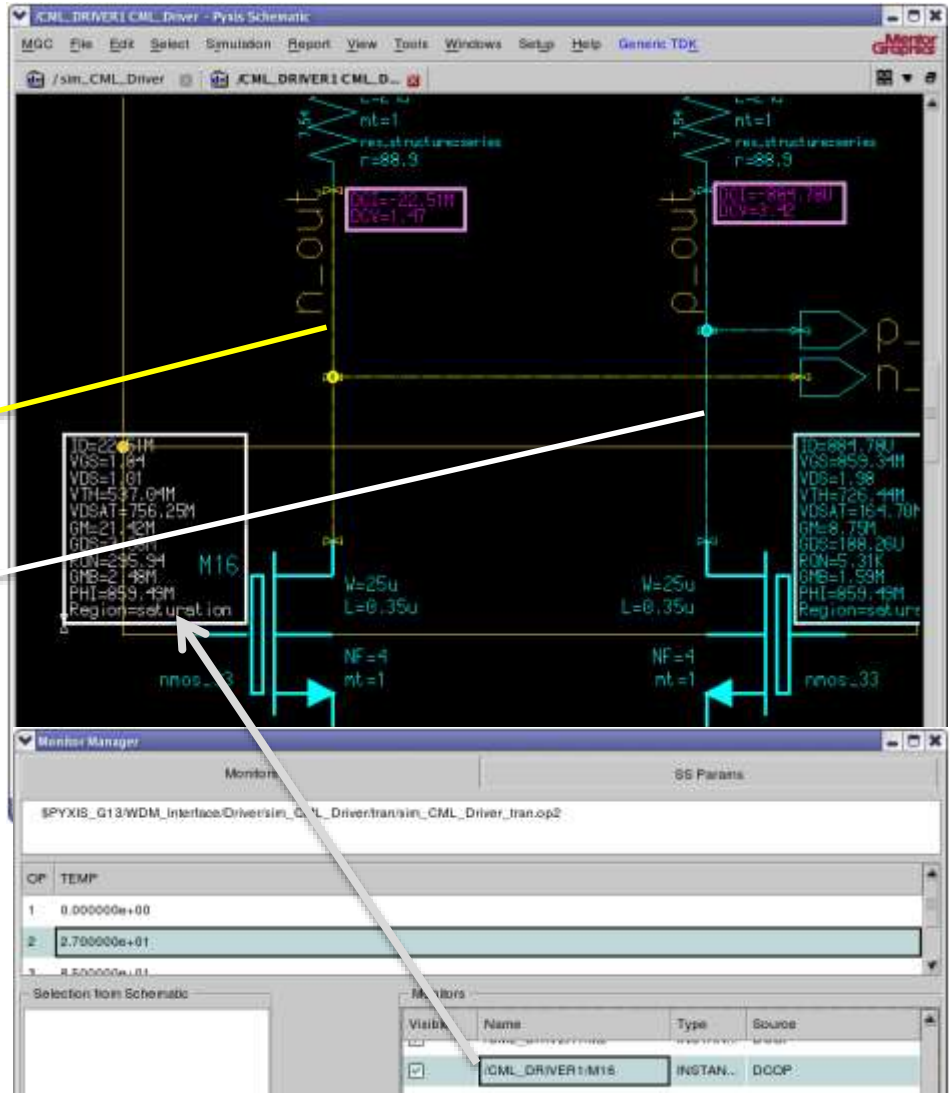


# Photonics + CMOS

## Post-simulation results analysis

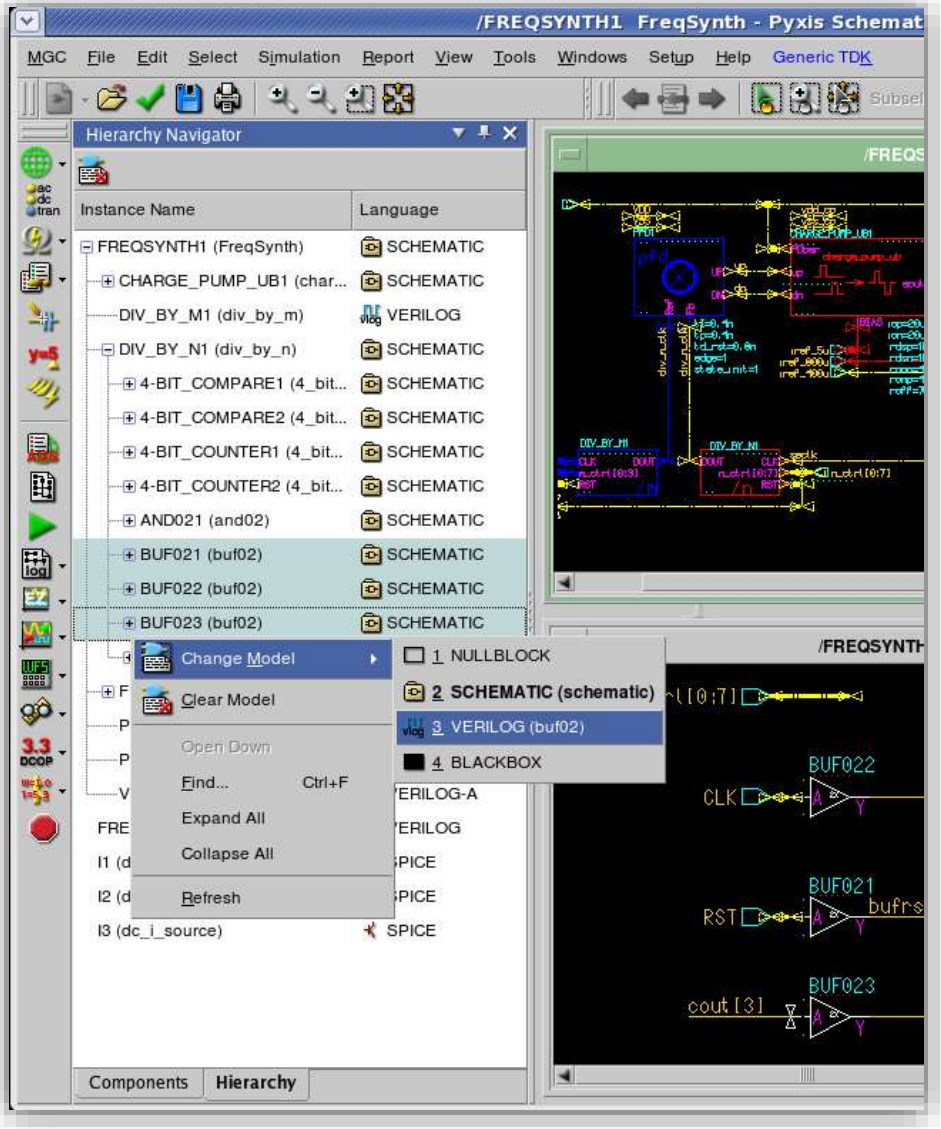
- Cross-probe to EZwave with matching color
- Annotate simulation values directly to schematic



# Photonics + CMOS

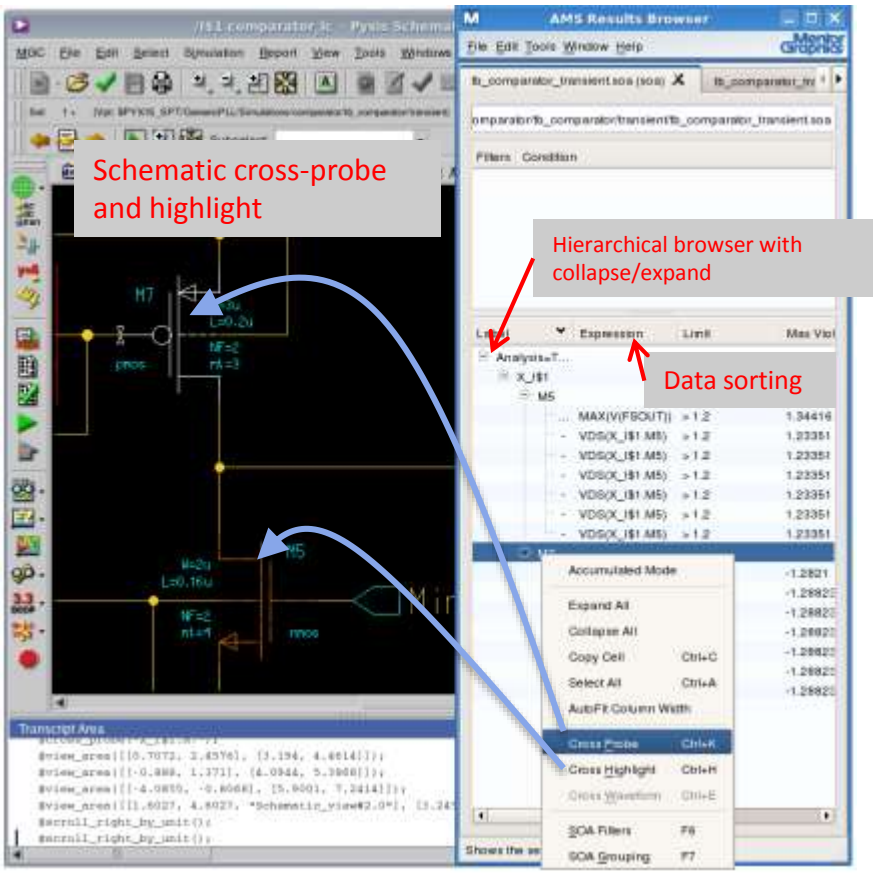
## Hierarchy based model configuration

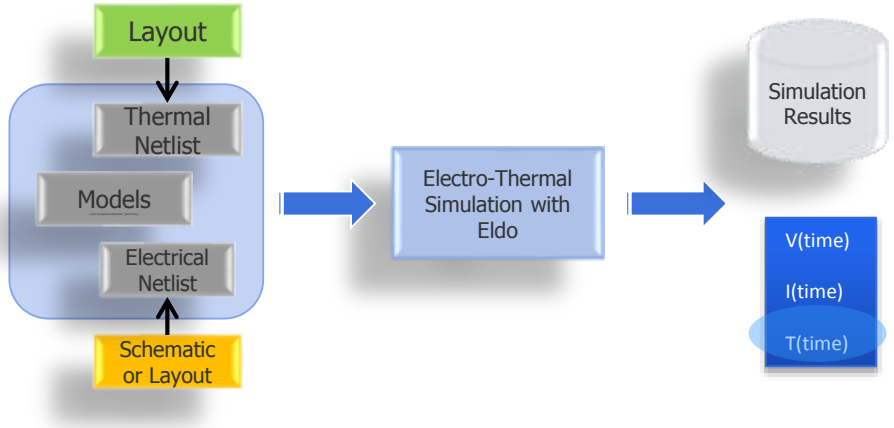



- Navigate by design hierarchy or by component listing
- Bidirectional cross selection between hierarchy navigator and schematic
- Configure models for multiple selected instances

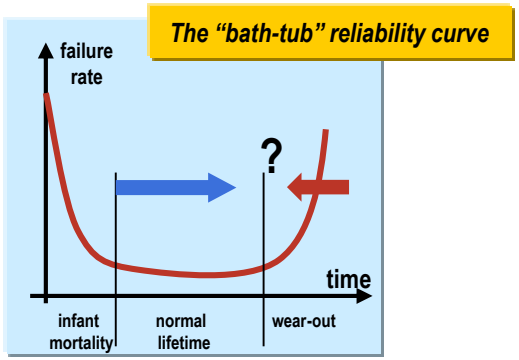
# Photonics + CMOS

## Diagnostic Simulation



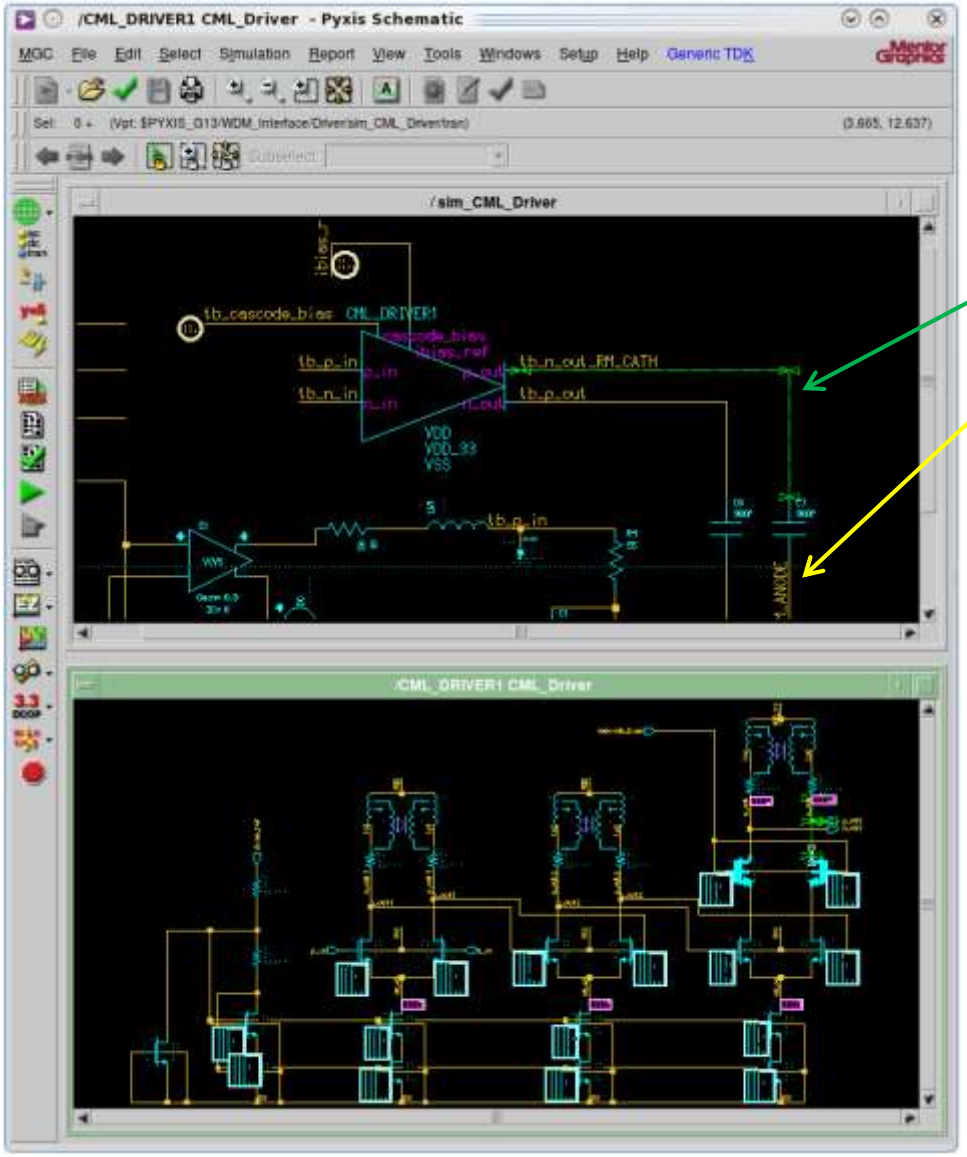




**Aging analysis: hot carrier and NBTI analysis -user definable models**

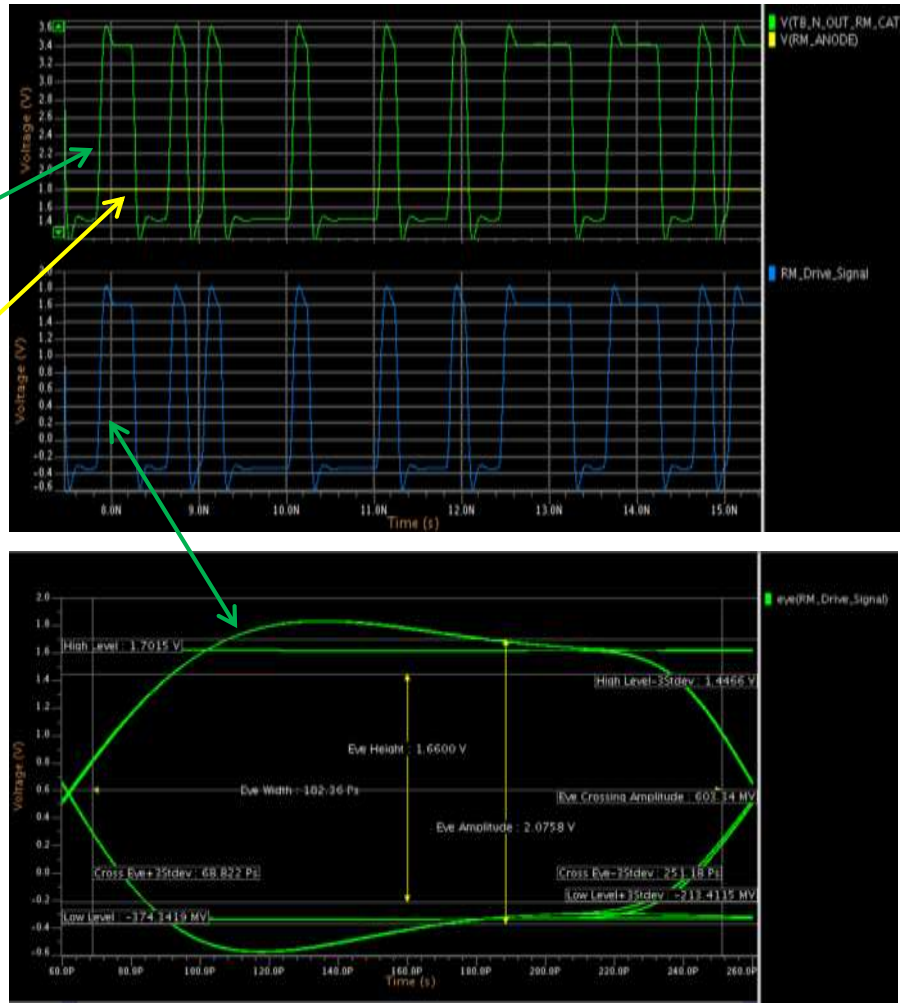


# Photonics + CMOS

## Generic13 CML Driver Example

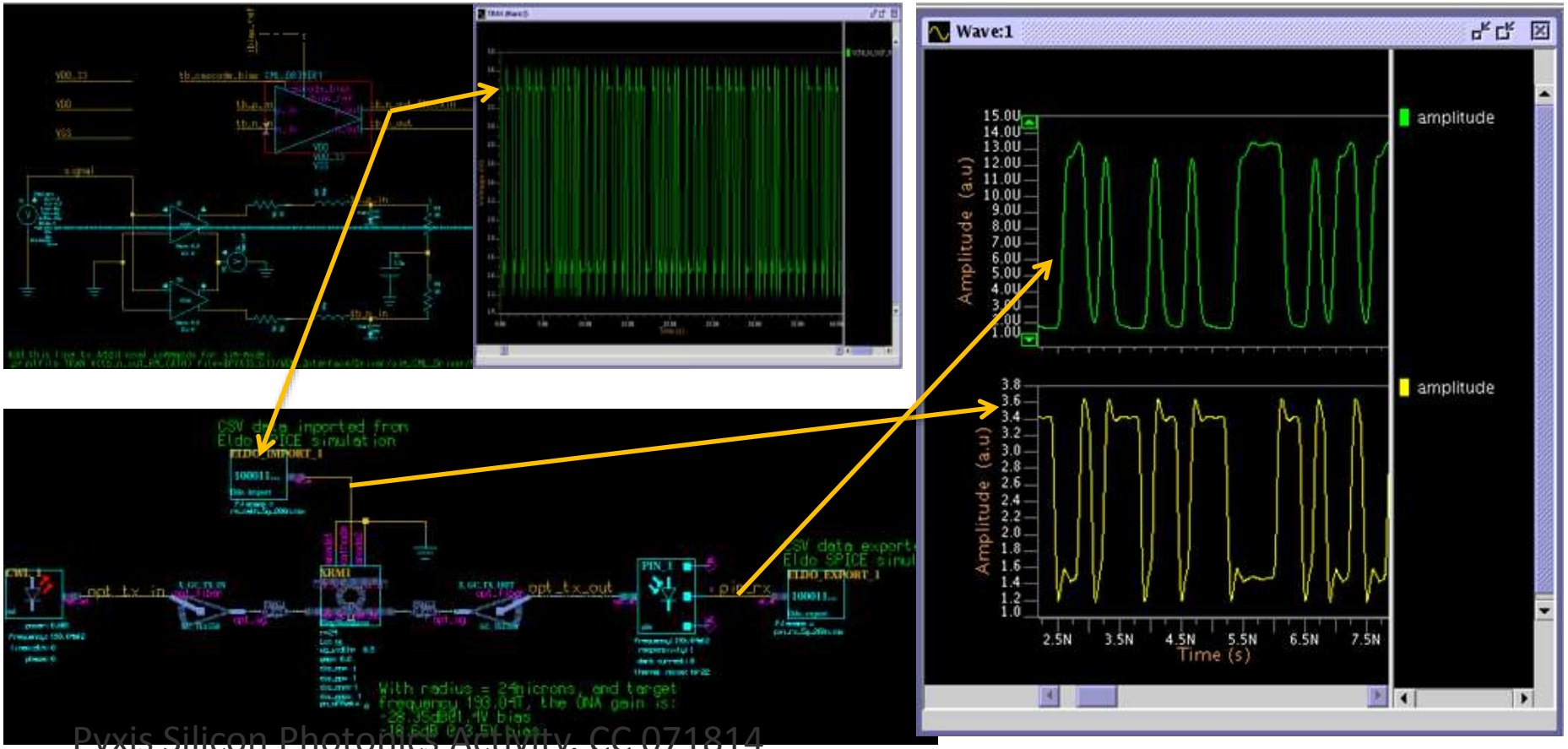



*Ring Modulator in reverse bias  equivalent capacitance ~300fF*



# Driving INTERCONNECT from Pyxis

- System level time domain simulation
  - ↗ User remains in Pyxis Schematic / EZwave cockpit for electrical and



# Photonics + CMOS

## Unified Post-Simulation Analysis in EZwave

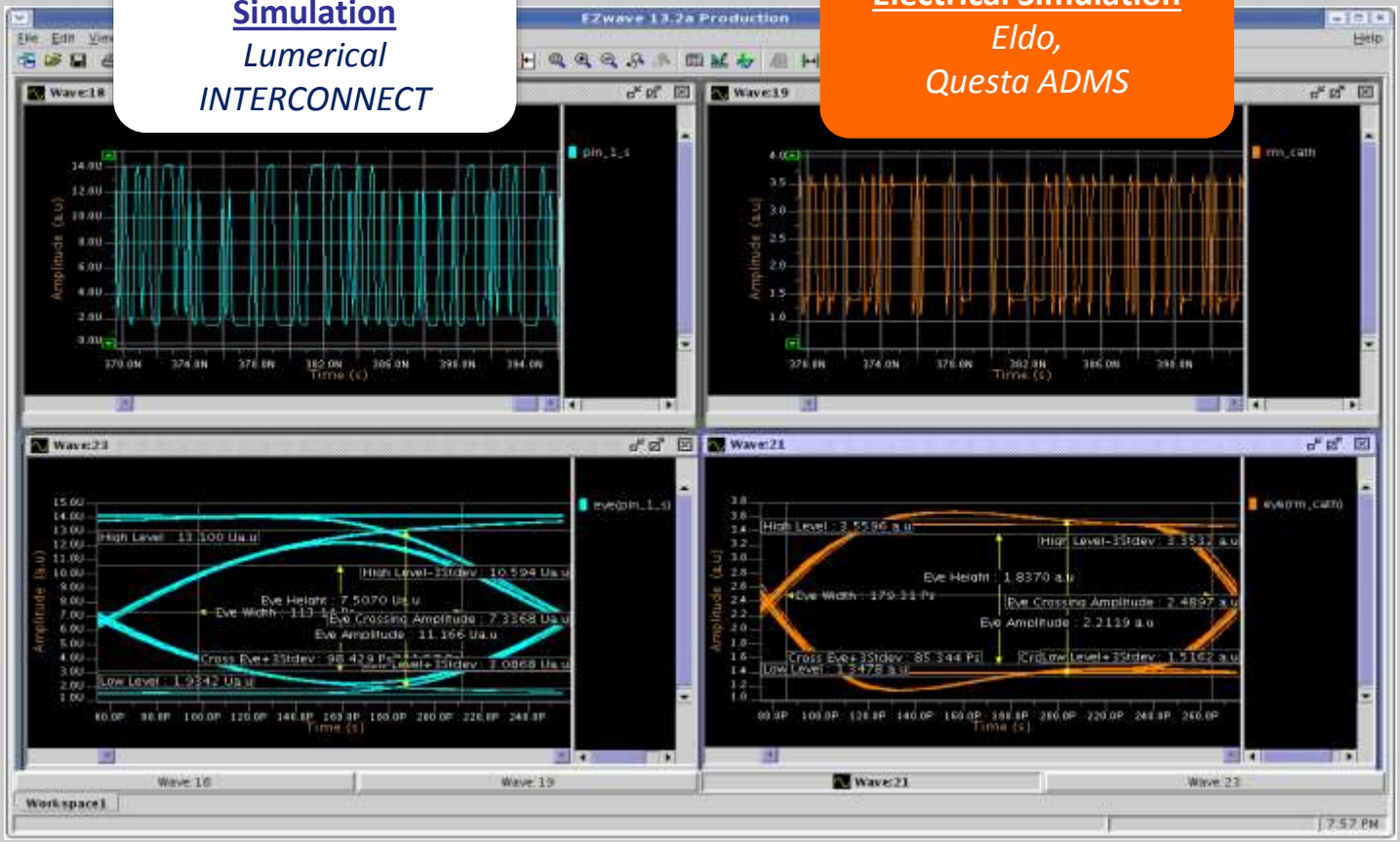
Mentor Graphics

lumerical illuminating the way

### Pyxis Schematic / EZwave Cockpit

**Photonic Circuit Simulation**
*Lumerical INTERCONNECT*

**Electrical Simulation**
*Eldo, Questa ADMS*



*A complete design flow for silicon photonics*

# *AVAILABLE PROCESS DESIGN KITS*

# PDKs for Silicon Photonics

- IME and IMEC Foundry PDKs (Available through CMC/Si-EPIC)
  - ↗ "designed to train undergraduate and graduate students and postdoctoral fellows across Canada in the new discipline of … (ICT) systems that involves miniaturization of optical components onto silicon chips"

NSERC CRSNG

Si-EPIC

CMC MICROSYSTEMS

http://siepic.ubc.ca

- ***Working directly with A*STAR IME to replace OpSIS offering***

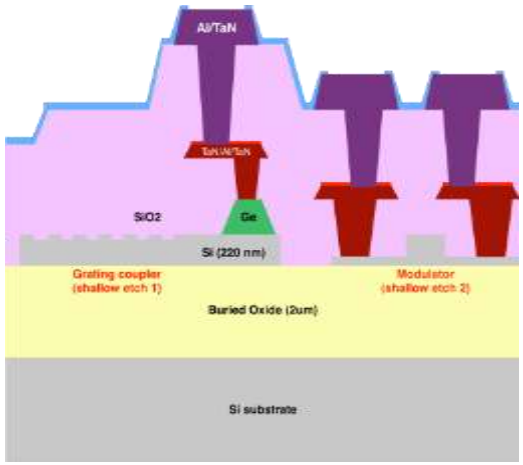
A*STAR IME

- IMEC (PDK in development)
  - ↗ Basic PDK available – working on full flow functionality

imec

**IME**

- Passives
- Modulators
- Detectors
- Edge / grating coupling



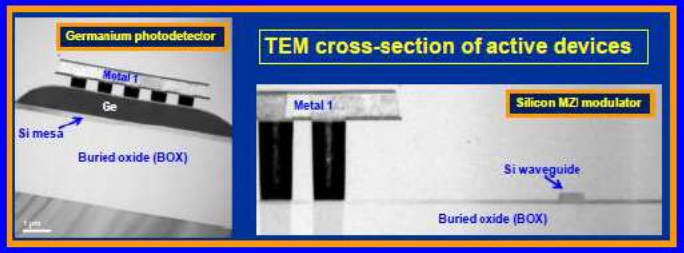
# PDKs for Silicon Photonics

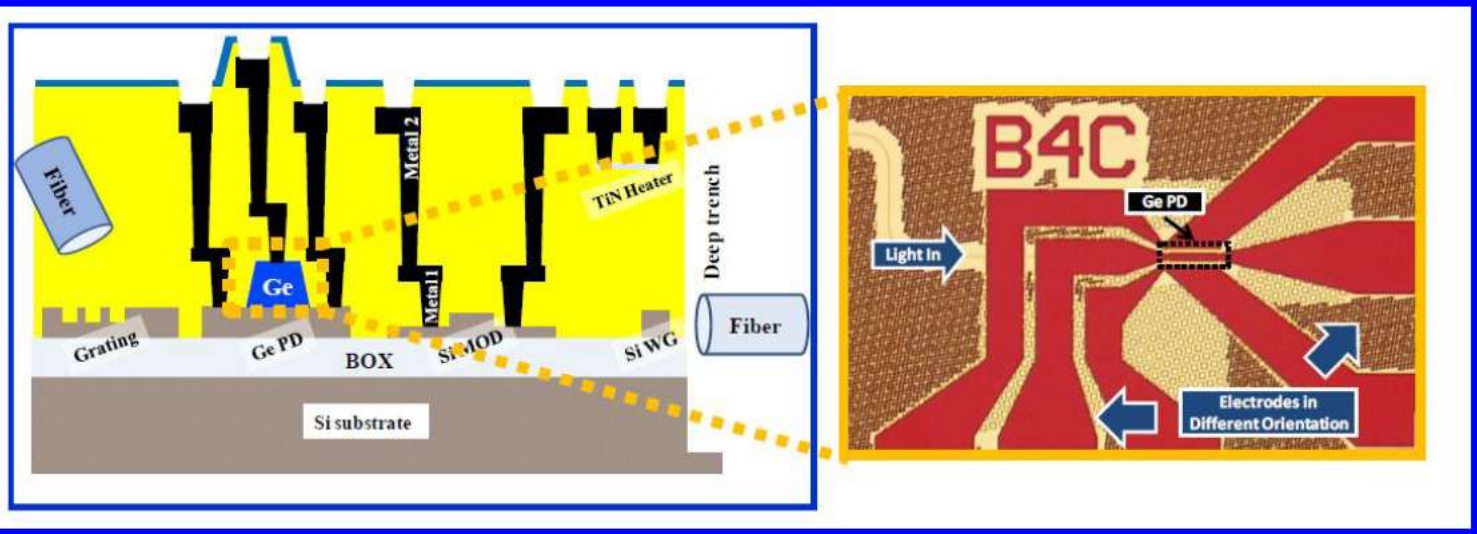
## IME's Silicon Photonics Process Platform

### Process overview

- 220nm Si/3 μm buried oxide (BOX) SOI
- Front-end process
  - 2 Si partial etches, 1 full etch to BOX
  - 6 implants for active devices
  - Ge epitaxial growth
- Backend process
  - 2 Al metal layers with W via plugs, TiN heater layer between the 2 metal layers
  - 120 μm deep Si trench

Photonic devices includes but not limited to Si passives (couplers, waveguides, crossings, splitters, bends, etc..), Si MZI MOD, Ge *pin* PD, and TiN heater

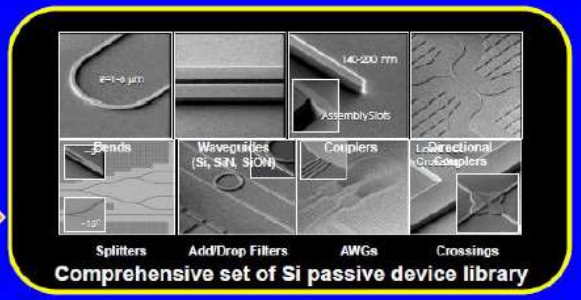


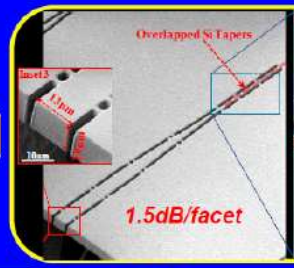
# PDKs for Silicon Photonics

## IME's Silicon Photonics Technology Overview

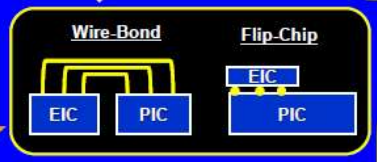
| Component | Description |
|---|---|
| SOI substrate | 220 nm Si/ 3000 nm buried oxide, 200 mm |
| Wavelength | 1310 nm (datacom), 1550 nm (telecom) |
| Passive devices | Routing, splitting, filtering, multiplexing, etc<br>e.g. WGs, splitters, directional couplers, MUX |
| Couplers | Fiber-to-chip coupling & vice versa,<br>e.g. vertical & edge |
| Heater | Thermal tuning, thermal modulation |
| Active devices | Modulating and detecting<br>e.g. Ge Photodetector and Si MZI Modulator |
| Electronics | Hybrid (Through wire bonding or flip-chip) |

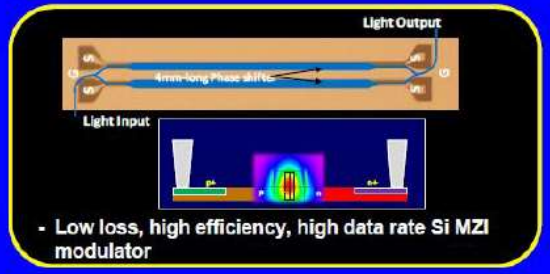



Comprehensive set of Si passive device library

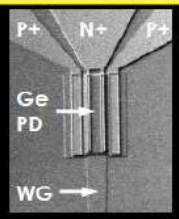



- Cantilevered mode-size convertor, Si nanotaper, Si 1-D, 2-D gratings
- Low loss, high alignment tolerance

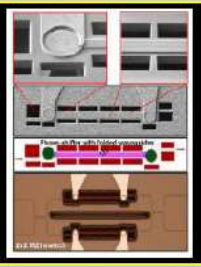



- Low loss, high efficiency, high data rate Si MZI modulator



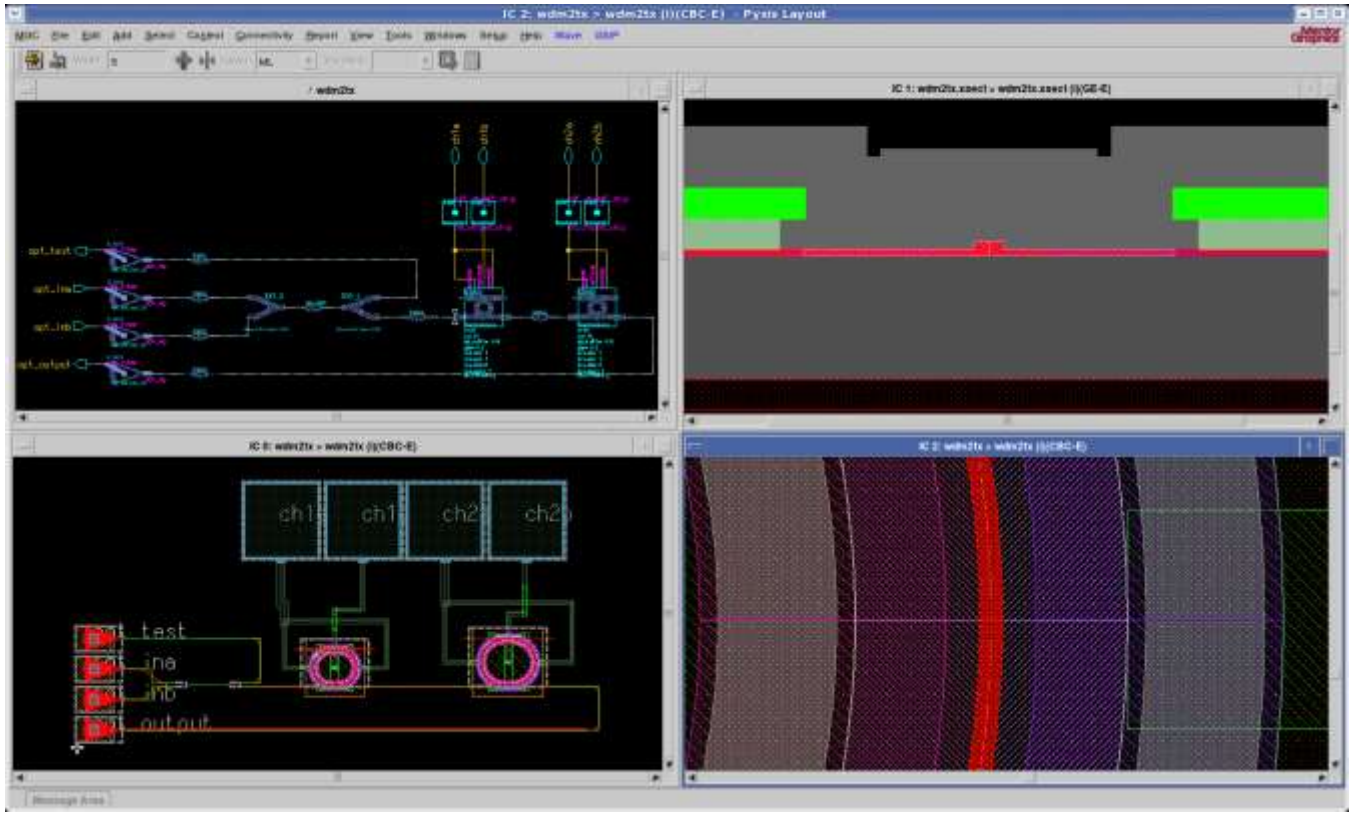

- Vertical pin Ge detectors with low dark current, high responsivity and high bandwidth



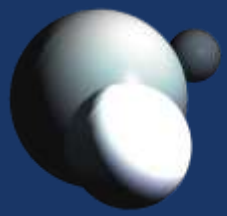
- High-Efficiency Integrated TO device for tuning, modulation of Switches, ring resonators;
- Thermal Isolation
- e.g., 2x2 MZI

# NDA neutral GSiP PDK with tutorials
## Available now!

- The Pyxis Wave reference packages provides extended features for Silicon Photonics PDK development
- Supports tiered custom PCell loading
- Waveguide routing enables full SDL flow




- Contains NDA neutral Silicon Photonics PDK created by University of British Columbia



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# THANK YOU!

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Cannes 2014